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Jameco Part Number 49912TI

# SN54192, SN54193, SN54LS192, SN54LS193, SN74192, SN74193, SN74LS192, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SDLS074 – DECEMBER 1972 – REVISED MARCH 1988

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

| TYPES          | TYPICAL MAXIMUM<br>COUNT FREQUENCY | TYPICAL<br>POWER DISSIPATION |
|----------------|------------------------------------|------------------------------|
| '192, '193     | 32 MHz                             | 325 mW                       |
| 'LS192, 'LS193 | 32 MHz                             | 95 mW                        |

## description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192 and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

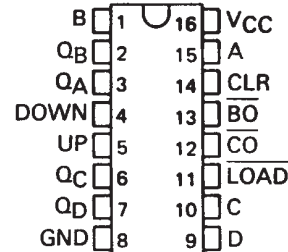
## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                       | SN54'      | SN54LS' | SN74'      | SN74LS' | UNIT |
|---------------------------------------|------------|---------|------------|---------|------|
| Supply voltage, $V_{CC}$ (see Note 1) | 7          | 7       | 7          | 7       | V    |
| Input voltage                         | 5.5        | 7       | 5.5        | 7       | V    |
| Operating free-air temperature range  | -55 to 125 |         | 0 to 70    |         | °C   |
| Storage temperature range             | -65 to 150 |         | -65 to 150 |         | °C   |

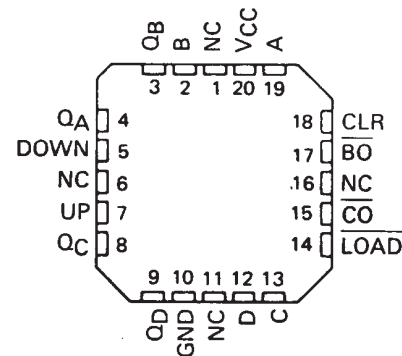
NOTE 1: Voltage values are with respect to network ground terminal.

SN54192, SN54193, SN54LS192,  
SN54LS193 . . . J OR W PACKAGE  
SN74192, SN74193 . . . N PACKAGE  
SN74LS192, SN74LS193 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS192, SN54LS193 . . . FK PACKAGE  
(TOP VIEW)



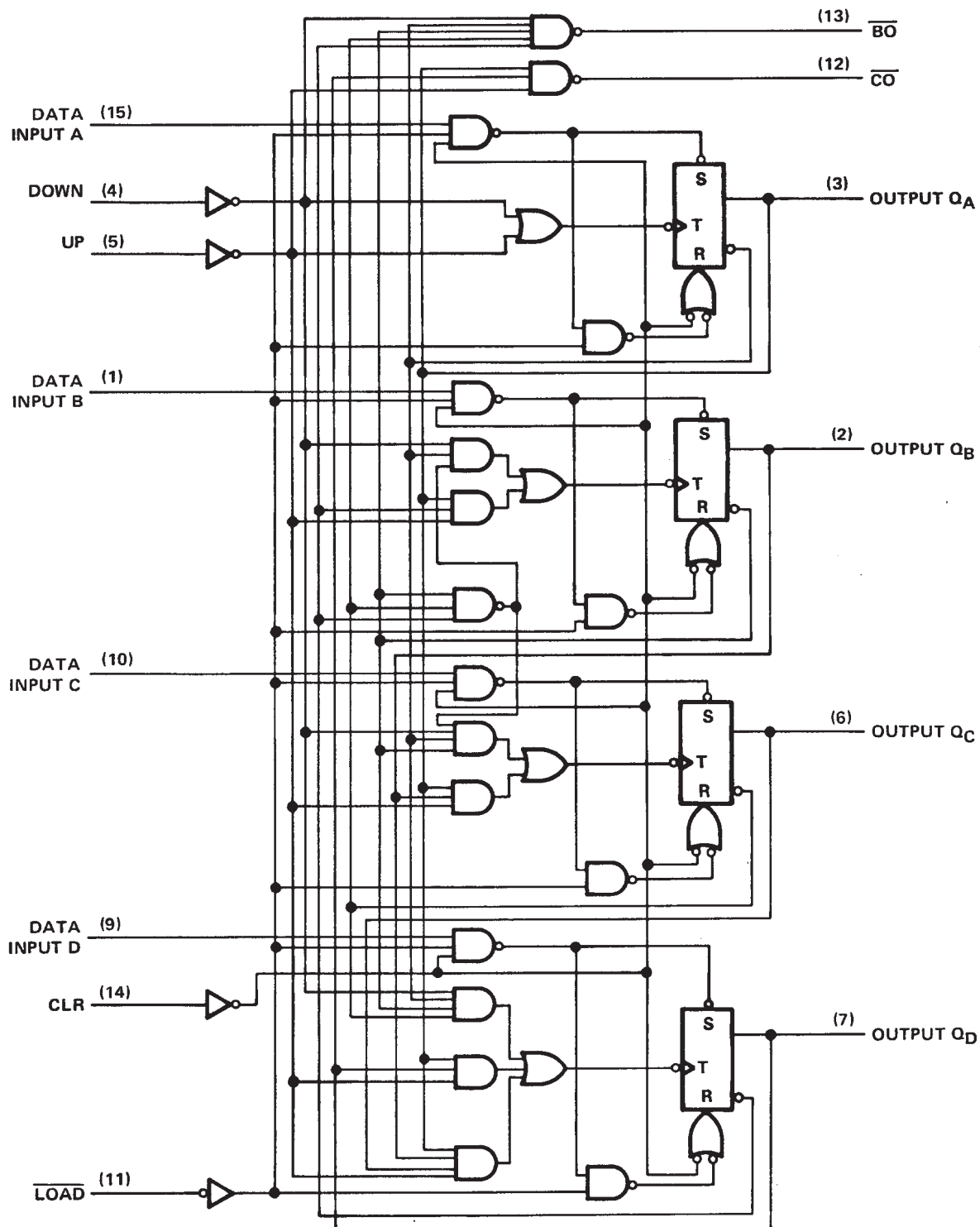
NC - No internal connection

# SN54192, SN54LS192, SN74192, SN74LS192

## SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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### logic diagram (positive logic)



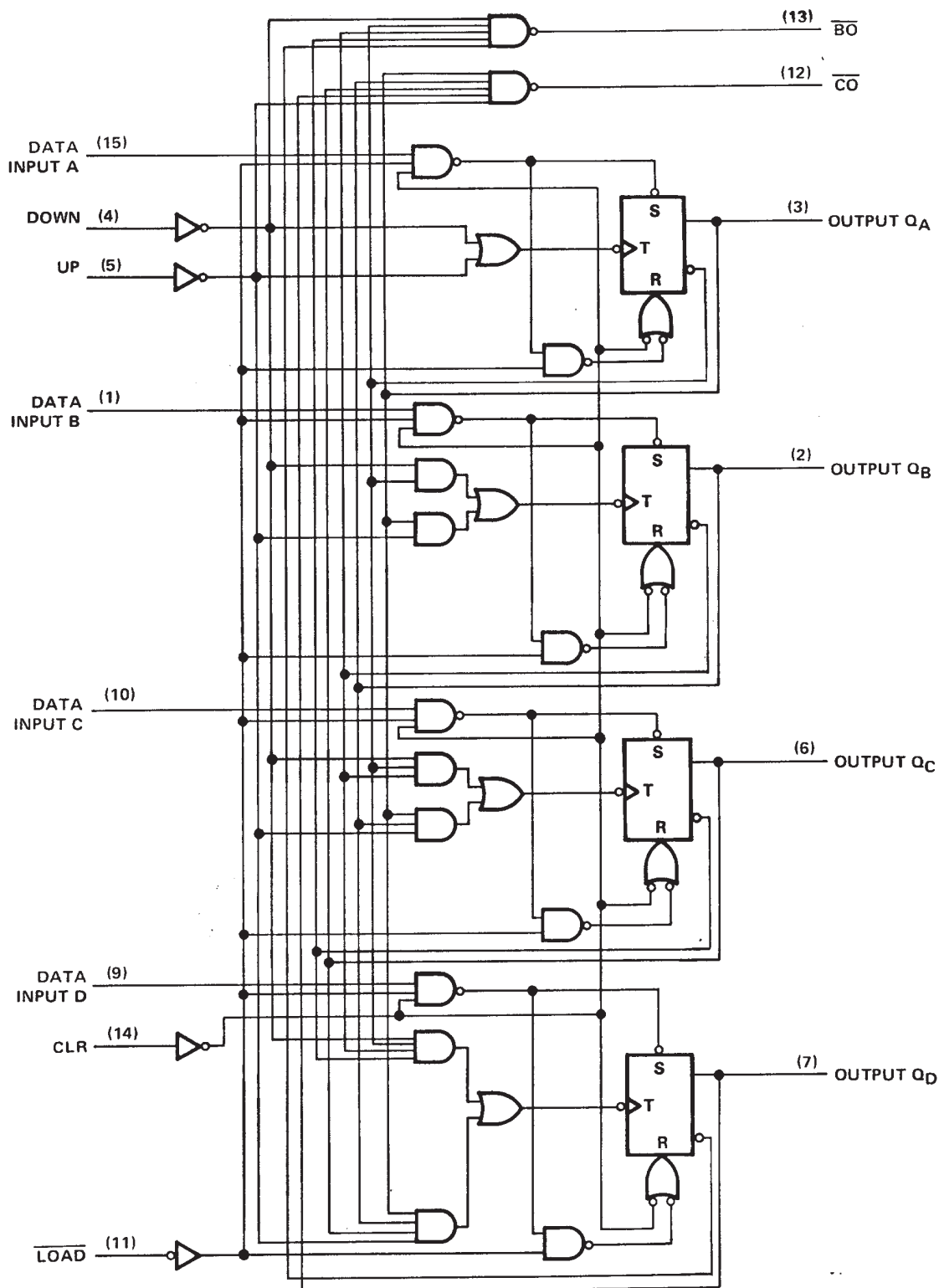
Pin numbers shown are for D, J, N, and W packages.

# SN54193, SN54LS193, SN74193, SN74LS193

## SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

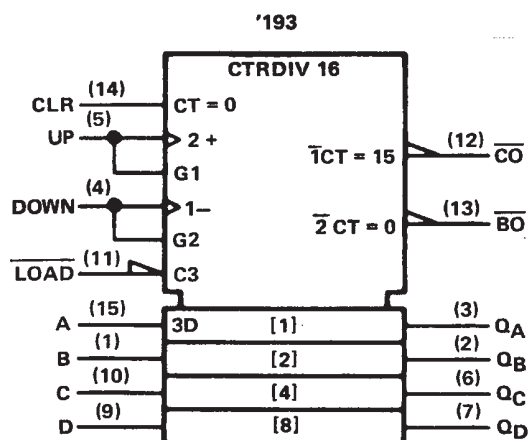
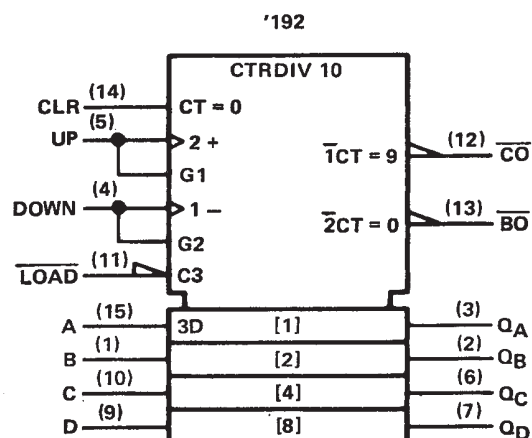


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SN54192, SN54193, SN54LS192, SN54LS193,  
SN74192, SN74193, SN74LS192, SN74LS193  
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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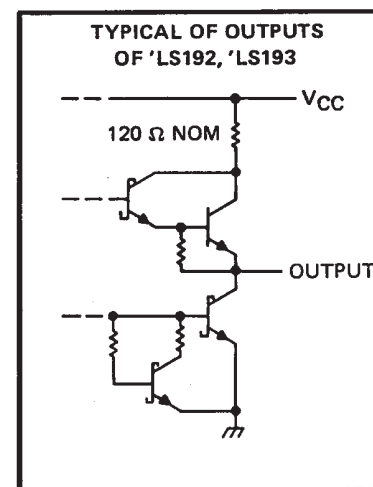
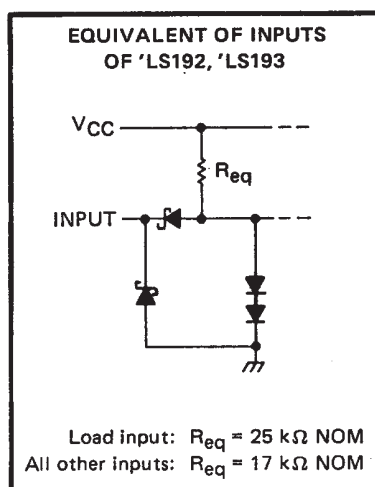
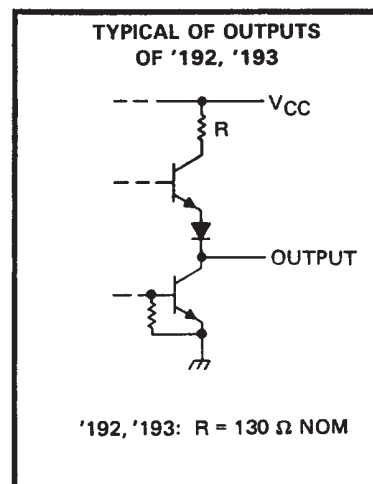
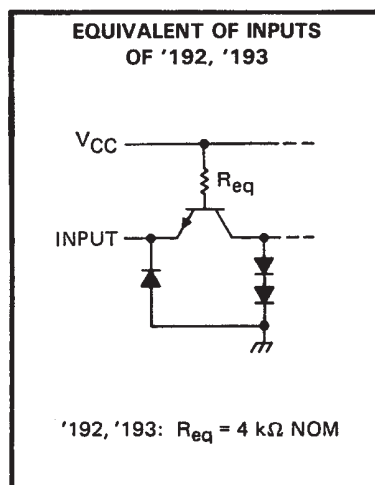
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



# SN54192, SN54LS192, SN74192, SN74LS192 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

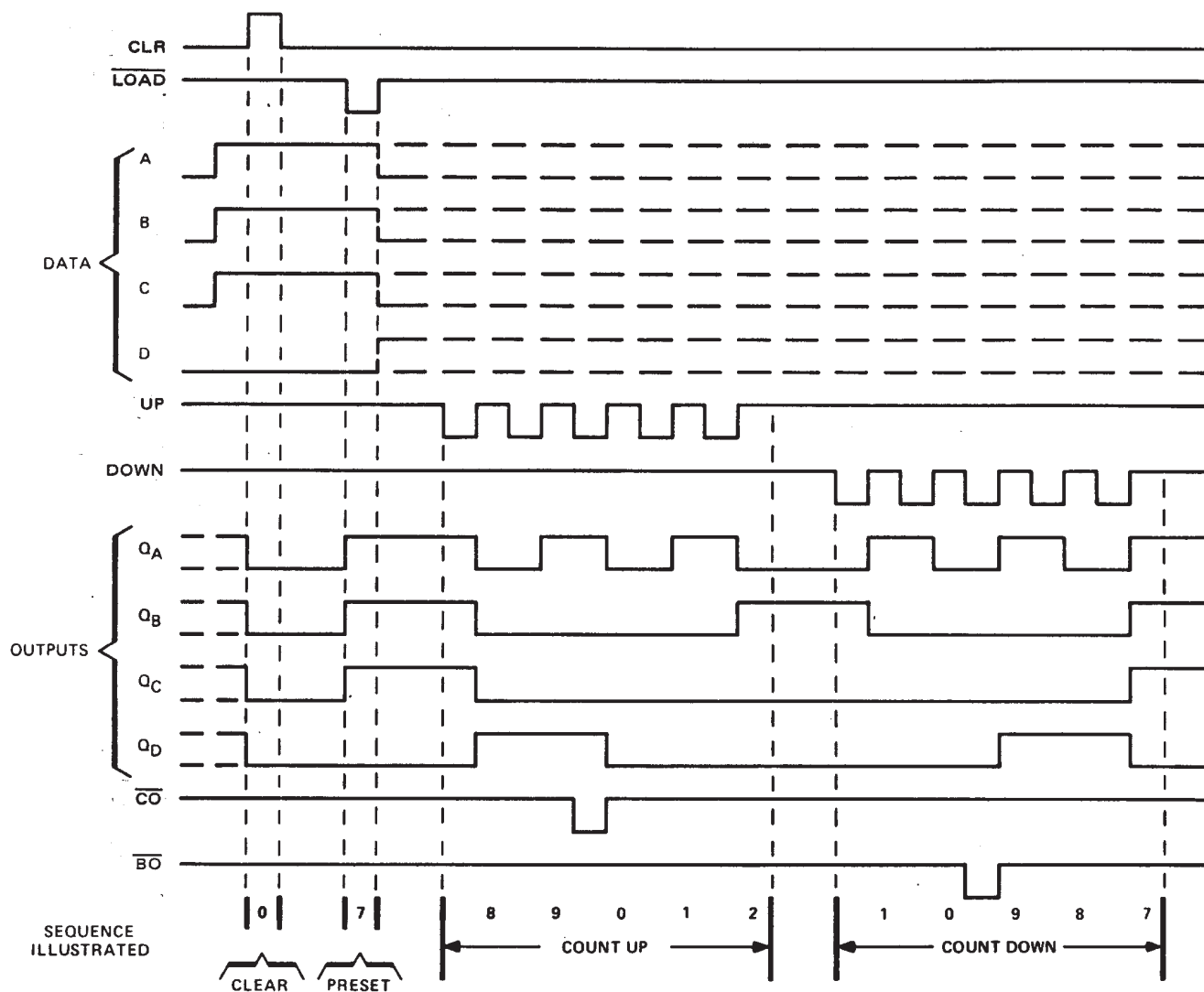
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## '192, 'LS192 DECADE COUNTERS

### typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.



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# SN54193, SN54LS193, SN74193, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

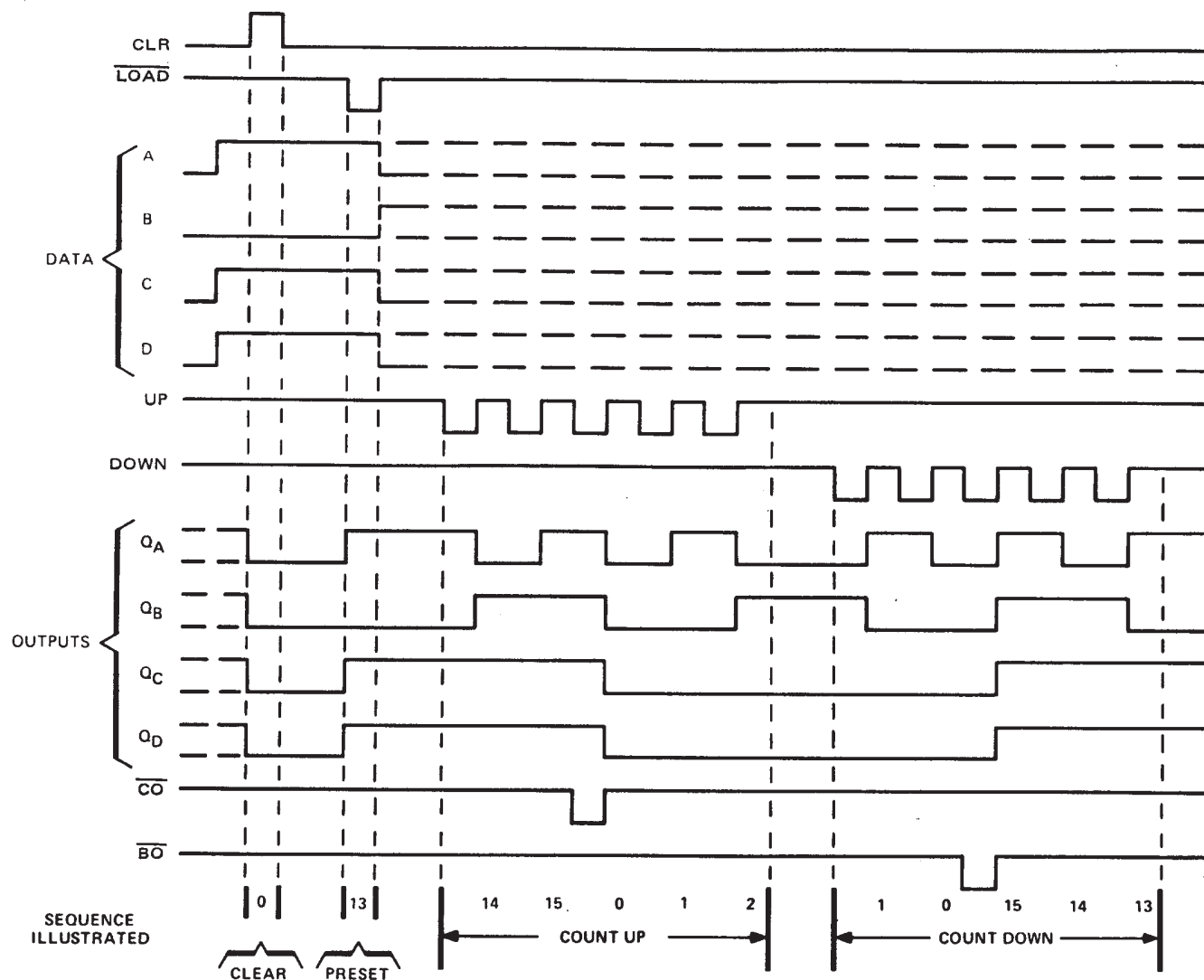
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## '193, 'LS193 BINARY COUNTERS

### typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.



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# SN54192, SN54193, SN74192, SN74193

## SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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### recommended operating conditions

|                    |                                 |                   | SN54192<br>SN54193 |     |     | SN74192<br>SN74193 |     |      | UNIT |
|--------------------|---------------------------------|-------------------|--------------------|-----|-----|--------------------|-----|------|------|
|                    |                                 |                   | MIN                | NOM | MAX | MIN                | NOM | MAX  |      |
| V <sub>CC</sub>    | Supply voltage                  |                   | 4.5                | 5   | 5.5 | 4.75               | 5   | 5.25 | V    |
| I <sub>OH</sub>    | High-level output current       |                   | −0.4               |     |     | −0.4               |     |      | mA   |
| I <sub>OL</sub>    | Low-level output current        |                   | 16                 |     |     | 16                 |     |      | mA   |
| f <sub>clock</sub> | Clock frequency                 |                   | 0                  | 25  |     | 0                  | 25  |      | MHz  |
| t <sub>w</sub>     | Width of any input pulse        |                   | 20                 |     |     | 20                 |     |      | ns   |
| t <sub>su</sub>    | Data setup time, (see Figure 1) |                   | 20                 |     |     | 20                 |     |      | ns   |
| t <sub>h</sub>     | Hold time                       | Data, high or low | 0                  |     |     | 0                  |     |      | ns   |
|                    |                                 | LOAD              | 3                  |     |     | 3                  |     |      |      |
| T <sub>A</sub>     | Operating free-air temperature  |                   | −55      125       |     |     | 0      70          |     |      | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       |                                        | TEST CONDITIONS†                                                                                    |  | SN54192<br>SN54193 |      |      | SN74192<br>SN74193 |      |      | UNIT |
|-----------------|----------------------------------------|-----------------------------------------------------------------------------------------------------|--|--------------------|------|------|--------------------|------|------|------|
|                 |                                        |                                                                                                     |  | MIN                | TYP‡ | MAX  | MIN                | TYP‡ | MAX  |      |
| V <sub>IH</sub> | High-level input voltage               |                                                                                                     |  | 2                  |      |      | 2                  |      |      | V    |
| V <sub>IL</sub> | Low-level input voltage                |                                                                                                     |  |                    |      | 0.8  |                    |      | 0.8  | V    |
| V <sub>IK</sub> | Input clamp voltage                    | V <sub>CC</sub> = MIN, I <sub>I</sub> = −12 mA                                                      |  |                    |      | −1.5 |                    |      | −1.5 | V    |
| V <sub>OH</sub> | High-level output voltage              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = −0.4 mA |  | 2.4                | 3.4  |      | 2.4                | 3.4  |      | V    |
| V <sub>OL</sub> | Low-level output voltage               | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA   |  |                    | 0.2  | 0.4  |                    | 0.2  | 0.4  | V    |
| I <sub>I</sub>  | Input current at maximum input voltage | V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V                                                       |  |                    |      | 1    |                    |      | 1    | mA   |
| I <sub>IH</sub> | High-level input current               | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V                                                       |  |                    |      | 40   |                    |      | 40   | μA   |
| I <sub>IL</sub> | Low-level input current                | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                                                       |  |                    |      | −1.6 |                    |      | −1.6 | mA   |
| I <sub>OS</sub> | Short-circuit output current§          | V <sub>CC</sub> = MAX                                                                               |  | −20                |      | −65  | −18                |      | −65  | mA   |
| I <sub>CC</sub> | Supply current                         | V <sub>CC</sub> = MAX, See Note 2                                                                   |  |                    | 65   | 89   |                    | 65   | 102  | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I<sub>CC</sub> is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER¶       | FROM<br>INPUT            | TO<br>OUTPUT           | TEST CONDITIONS                                                           | MIN | TYP | MAX | UNIT |
|------------------|--------------------------|------------------------|---------------------------------------------------------------------------|-----|-----|-----|------|
| f <sub>max</sub> |                          |                        | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 400 Ω,<br>See Figures 1 and 2 | 25  | 32  |     | MHz  |
| t <sub>PLH</sub> | UP                       | $\overline{\text{CO}}$ |                                                                           |     | 17  | 26  | ns   |
| t <sub>PHL</sub> |                          |                        |                                                                           |     | 16  | 24  |      |
| t <sub>PLH</sub> | DOWN                     | $\overline{\text{BO}}$ |                                                                           |     | 16  | 24  | ns   |
| t <sub>PHL</sub> |                          |                        |                                                                           |     | 16  | 24  |      |
| t <sub>PLH</sub> | UP OR DOWN               | Q                      |                                                                           |     | 25  | 38  | ns   |
| t <sub>PHL</sub> |                          |                        |                                                                           |     | 31  | 47  |      |
| t <sub>PLH</sub> | $\overline{\text{LOAD}}$ | Q                      |                                                                           |     | 27  | 40  | ns   |
| t <sub>PHL</sub> |                          |                        |                                                                           |     | 29  | 40  |      |
| t <sub>PHL</sub> | CLR                      | Q                      |                                                                           |     | 22  | 35  | ns   |

¶ f<sub>max</sub> ≡ maximum clock frequency

t<sub>PLH</sub> ≡ propagation delay time, low-to-high-level output

t<sub>PHL</sub> ≡ propagation delay time, high-to-low-level output



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# SN54LS192, SN54LS193, SN74LS192, SN74LS193

## SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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### recommended operating conditions

|                    |                                      | SN54LS192<br>SN54LS193 |     |      | SN74LS192<br>SN74LS193 |     |      | UNIT |
|--------------------|--------------------------------------|------------------------|-----|------|------------------------|-----|------|------|
|                    |                                      | MIN                    | NOM | MAX  | MIN                    | NOM | MAX  |      |
| V <sub>CC</sub>    | Supply voltage                       | 4.5                    | 5   | 5.5  | 4.75                   | 5   | 5.25 | V    |
| I <sub>OH</sub>    | High-level output current            |                        |     | −400 |                        |     | −400 | μA   |
| I <sub>OL</sub>    | Low-level output current             |                        |     | 4    |                        |     | 8    | mA   |
| f <sub>clock</sub> | Clock frequency                      | 0                      |     | 25   | 0                      |     | 25   | MHz  |
| t <sub>w</sub>     | Width of any input pulse             | 20                     |     |      | 20                     |     |      | ns   |
| t <sub>su</sub>    | Clear inactive-state setup time      | 15                     |     |      | 15                     |     |      | ns   |
|                    | Load inactive-state setup time       | 15                     |     |      | 15                     |     |      | ns   |
|                    | Data setup time (see Figure 1)       | 20                     |     |      | 20                     |     |      | ns   |
| t <sub>h</sub>     | Data hold time                       | 5                      |     |      | 5                      |     |      | ns   |
| T <sub>A</sub>     | Operating free-air temperature range | −55                    |     | 125  | 0                      |     | 70   | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                             | TEST CONDITIONS†                                                                                                  | SN54LS192<br>SN54LS193 |      |      | SN74LS192<br>SN74LS193 |      |     | UNIT |
|-------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|------------------------|------|------|------------------------|------|-----|------|
|                                                       |                                                                                                                   | MIN                    | TYP‡ | MAX  | MIN                    | TYP‡ | MAX |      |
| V <sub>IH</sub> High-level input voltage              |                                                                                                                   | 2                      |      |      | 2                      |      |     | V    |
| V <sub>IL</sub> Low-level input voltage               |                                                                                                                   | 0.7                    |      |      | 0.8                    |      |     | V    |
| V <sub>IK</sub> Input clamp voltage                   | V <sub>CC</sub> = MIN, I <sub>I</sub> = −18 mA                                                                    | −1.5                   |      |      | −1.5                   |      |     | V    |
| V <sub>OH</sub> High-level output voltage             | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = −400 μA | 2.5                    | 3.4  |      | 2.7                    | 3.4  |     | V    |
| V <sub>OL</sub> Low-level output voltage              | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max                            | I <sub>OL</sub> = 4 mA |      | 0.25 | 0.4                    | 0.15 | 0.4 | V    |
|                                                       |                                                                                                                   | I <sub>OL</sub> = 8 mA |      |      |                        | 0.35 | 0.5 |      |
| I <sub>I</sub> Input current at maximum input voltage | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V                                                                       | 0.1                    |      |      | 0.1                    |      |     | mA   |
| I <sub>IH</sub> High-level input current              | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                                                                     | 20                     |      |      | 20                     |      |     | μA   |
| I <sub>IL</sub> Low-level input current               | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                                                                     | −0.4                   |      |      | −0.4                   |      |     | mA   |
| I <sub>OS</sub> Short-circuit output current§         | V <sub>CC</sub> = MAX                                                                                             | −20                    | −100 |      | −20                    | −100 |     | mA   |
| I <sub>CC</sub> Supply current                        | V <sub>CC</sub> = MAX, See Note 2                                                                                 | 19                     | 34   |      | 19                     | 34   |     | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I<sub>CC</sub> is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

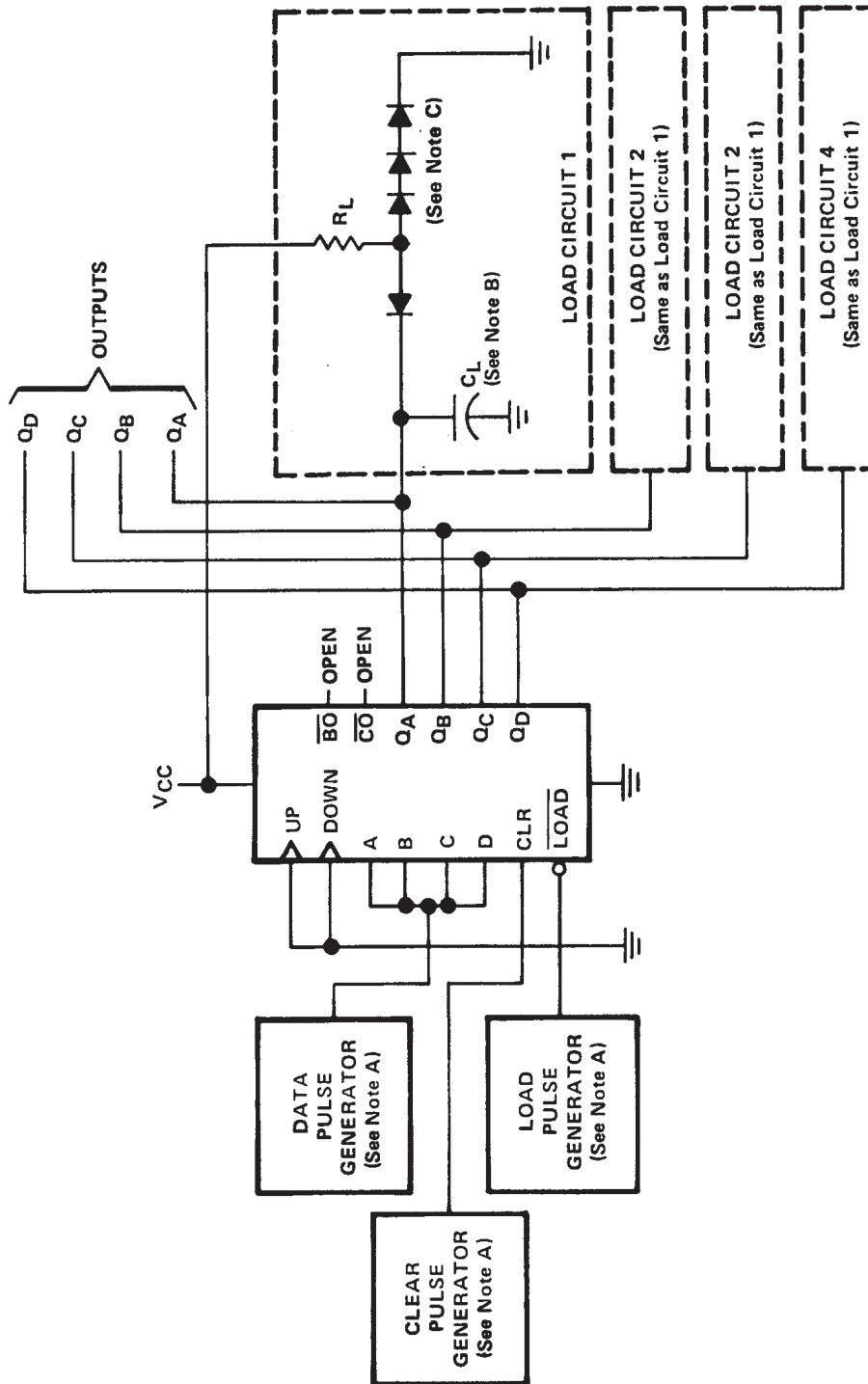
| PARAMETER        | FROM INPUT        | TO OUTPUT       | TEST CONDITIONS                                                          | MIN | TYP | MAX | UNIT |
|------------------|-------------------|-----------------|--------------------------------------------------------------------------|-----|-----|-----|------|
| f <sub>max</sub> |                   |                 | C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 2 kΩ,<br>See Figures 1 and 2 | 25  | 32  |     | MHz  |
| t <sub>PLH</sub> | UP                | $\overline{CO}$ |                                                                          |     | 17  | 26  | ns   |
| t <sub>PHL</sub> |                   |                 |                                                                          |     | 18  | 24  |      |
| t <sub>PLH</sub> | DOWN              | $\overline{BO}$ |                                                                          |     | 16  | 24  | ns   |
| t <sub>PHL</sub> |                   |                 |                                                                          |     | 15  | 24  |      |
| t <sub>PLH</sub> | UP OR DOWN        | Q               |                                                                          |     | 27  | 38  | ns   |
| t <sub>PHL</sub> |                   |                 |                                                                          |     | 30  | 47  |      |
| t <sub>PLH</sub> | $\overline{LOAD}$ | Q               |                                                                          |     | 24  | 40  | ns   |
| t <sub>PHL</sub> |                   |                 |                                                                          |     | 25  | 40  |      |
| t <sub>PHL</sub> | CLR               | Q               |                                                                          |     | 23  | 35  | ns   |



SN54192, SN54193, SN54LS192, SN54LS193,  
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SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

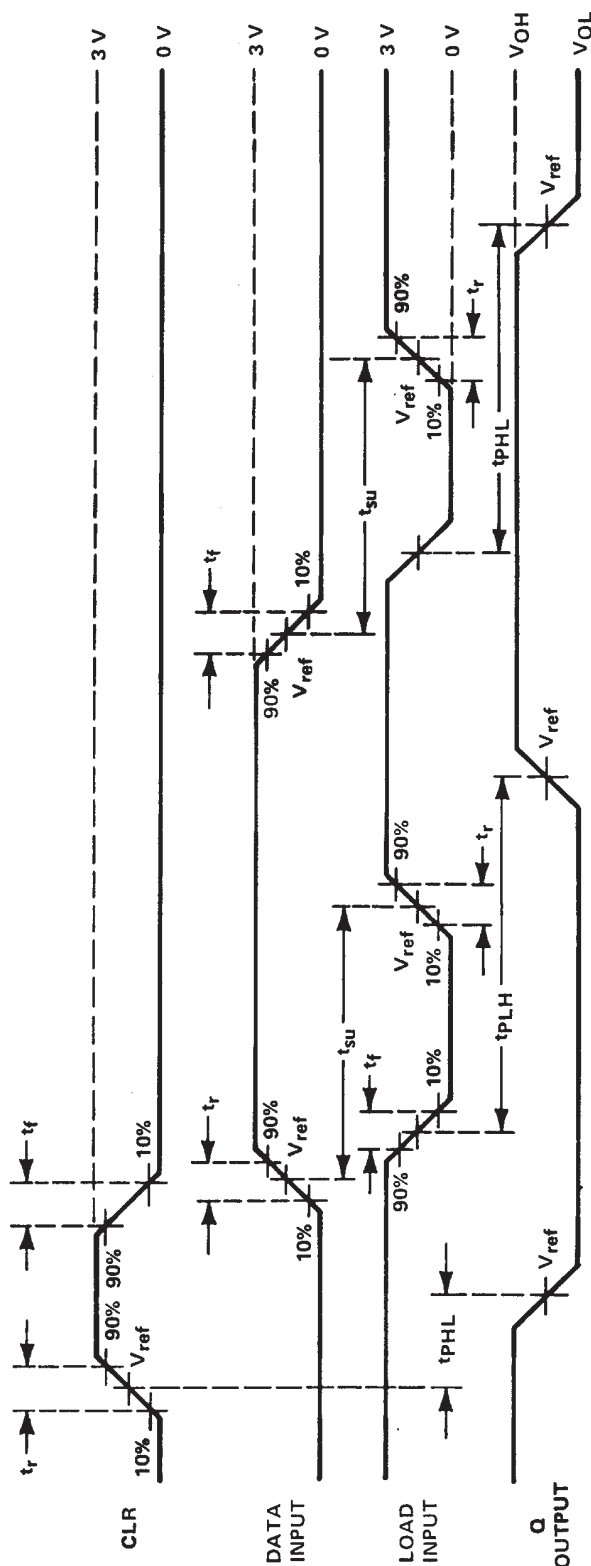
- NOTES: A. The pulse generators have the following characteristics:  $Z_{out} \approx 50 \Omega$  and for the data pulse generator  $PRR \leq 500 \text{ kHz}$ , duty cycle = 50%; for the load pulse generator  $PRR$  is two times data  $PRR$ , duty cycle = 50%.
- B.  $C_L$  includes probe and jig capacitance.
- C. Diodes are 1N3064 or equivalent.
- D.  $t_r$  and  $t_f \leq 7 \text{ ns}$ .
- E.  $V_{ref}$  is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 1A – CLEAR, SETUP AND LOAD TIMES

SN54192, SN54193, SN54LS192, SN54LS193,  
SN74192, SN74193, SN74LS192, SN74LS193  
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics:  $Z_{out} \approx 50 \Omega$  and for the data pulse generator PRR  $\leq 500$  kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
- B.  $C_L$  includes probe and jig capacitance.
- C. Diodes are 1N3064 or equivalent.
- D.  $t_r$  and  $t_f \leq 7$  ns.
- E.  $V_{ref}$  is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

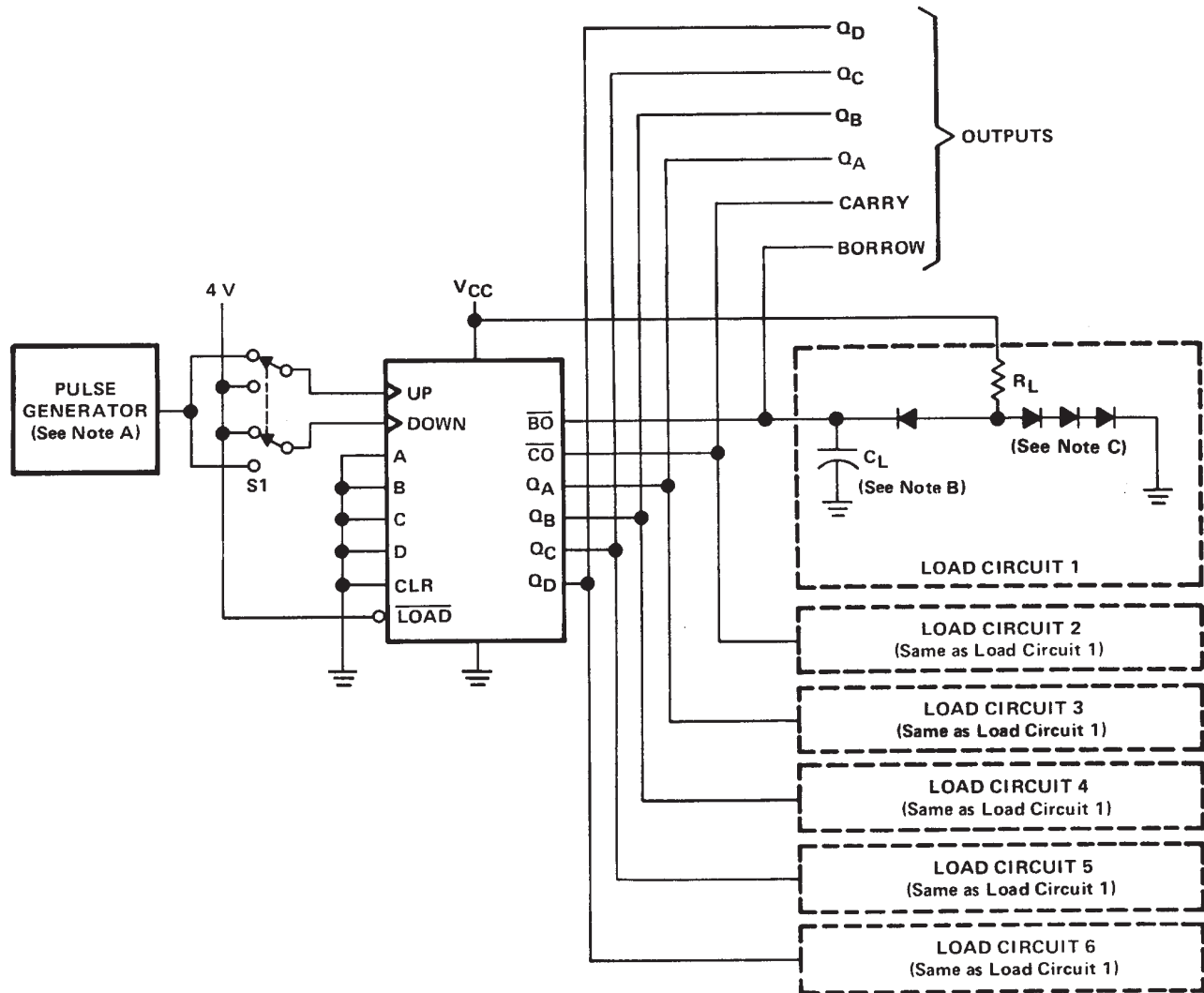
FIGURE 1B – CLEAR, SETUP, AND LOAD TIMES

SN54192, SN54193, SN54LS192, SN54LS193,  
SN74192, SN74193, SN74LS192, SN74LS193

# SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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## PARAMETER MEASUREMENT INFORMATION



### TEST CIRCUIT

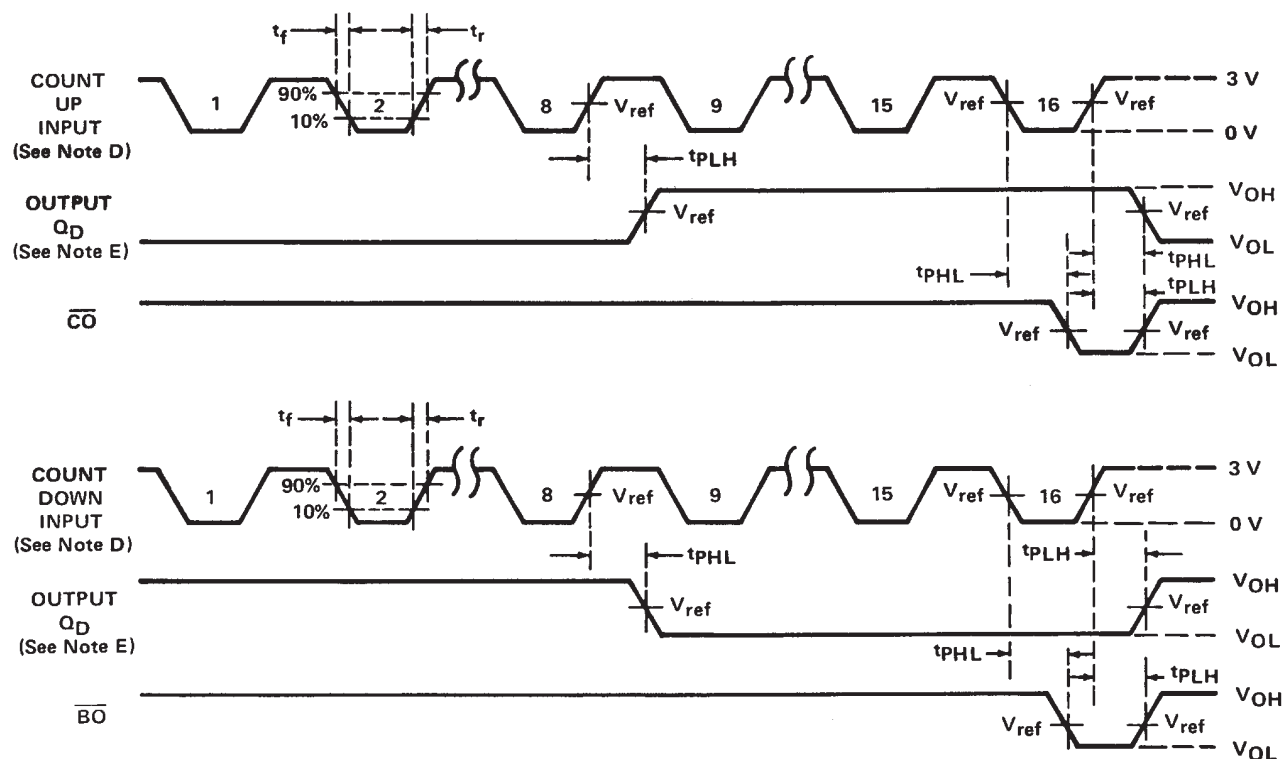
- NOTES: A. The pulse generators have the following characteristics:  $PRR \approx 1 \text{ MHz}$ ,  $Z_{out} \approx 50 \Omega$ , duty cycle = 50%.
- B.  $C_L$  includes probe and jig capacitance.
- C. Diodes are 1N3064 or equivalent.
- D. Count-up and count-down pulse shown are for the '193 and 'LS193 binary counters. Count cycle for '192 and 'LS192 decade counters is 1 through 10.
- E. Waveforms for outputs  $Q_A$ ,  $Q_B$ , and  $Q_C$  are omitted to simplify the drawing.
- F.  $t_r$  and  $t_f \leq 7 \text{ ns}$ .
- G.  $V_{ref}$  is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 2A – PROPAGATION DELAY TIMES

SN54192, SN54193, SN54LS192, SN54LS193,  
 SN74192, SN74193, SN74LS192, SN74LS193  
 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

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PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generators have the following characteristics: PRR  $\approx$  1 MHz,  $Z_{out} \approx 50 \Omega$ , duty cycle = 50%.  
 B.  $C_L$  includes probe and jig capacitance.  
 C. Diodes are 1N3064 or equivalent.  
 D. Count-up and count-down pulse shown are for the '193 and 'LS193 binary counters. Count cycle for '192 and 'LS192 decade counters is 1 through 10.  
 E. Waveforms for outputs  $Q_A$ ,  $Q_B$ , and  $Q_C$  are omitted to simplify the drawing.  
 F.  $t_r$  and  $t_f \leq 7$  ns.  
 G.  $V_{ref}$  is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 2B – PROPAGATION DELAY TIMES

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