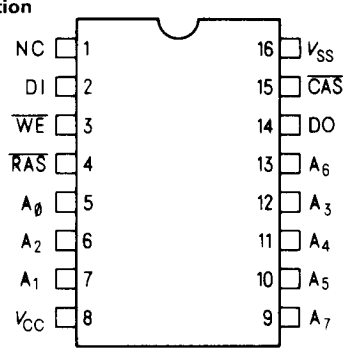
Jameco Part Number 41662SIEMENS

SIEMENS

HYB 4164-1, HYB 4164-2, HYB 4164-3
65,536-Bit Dynamic Random Access Memory (RAM)

- 65,536 X1 bit organization
- Industry standard 16-pin JEDEC configuration
- Single +5 V ±10% power supply
- Low power dissipation
  - 150 mW active (max.)
  - 20 mW standby (max.)
- 120 ns access time,
  220 ns cycle (HYB 4164-1)
  150 ns access time,
  280 ns cycle (HYB 4164-2)
  200 ns access time,
  330 ns cycle (HYB 4164-3)
- All inputs and outputs TTL compatible
- High over- and undershooting capability on all inputs
- Low supply current transients
- $\overline{CAS}$ controlled output providing latched or unlatched data
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, hidden refresh
- 256 refresh cycles with 4 ms long refresh period
- Page Mode Read and Write

Pin Configuration



Pin Names	
$A_0 - A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data In
NC	No Connection
DO	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground (0 V)

The HYB 4164 is a 65536-words by 1-bit, MOS random access memory circuit fabricated with Siemens new 5-Volt only n-channel silicon gate technology, using double layer polysilicon. To protect the chip against α-radiation a Siemens proprietary chip cover is used. The HYB 4164 uses single transistor dynamic storage cells and dynamic control circuitry to achieve high speed at very low power dissipation.
Multiplexed address inputs permit the HYB 4164 to be packaged in an industry standard 16-pin dual-in-line package.

System oriented features include single power supply with ±10% tolerance, on-chip address and data latches which eliminate the need for interface registers and fully TTL compatible inputs and outputs, including clocks.
In addition to the usual read, write and read-modify-write cycles, the HYB 4164 is capable of early and delayed write cycles, $\overline{RAS}$-only refresh and hidden refresh. Common I/O capability is given by using "early write" operation.

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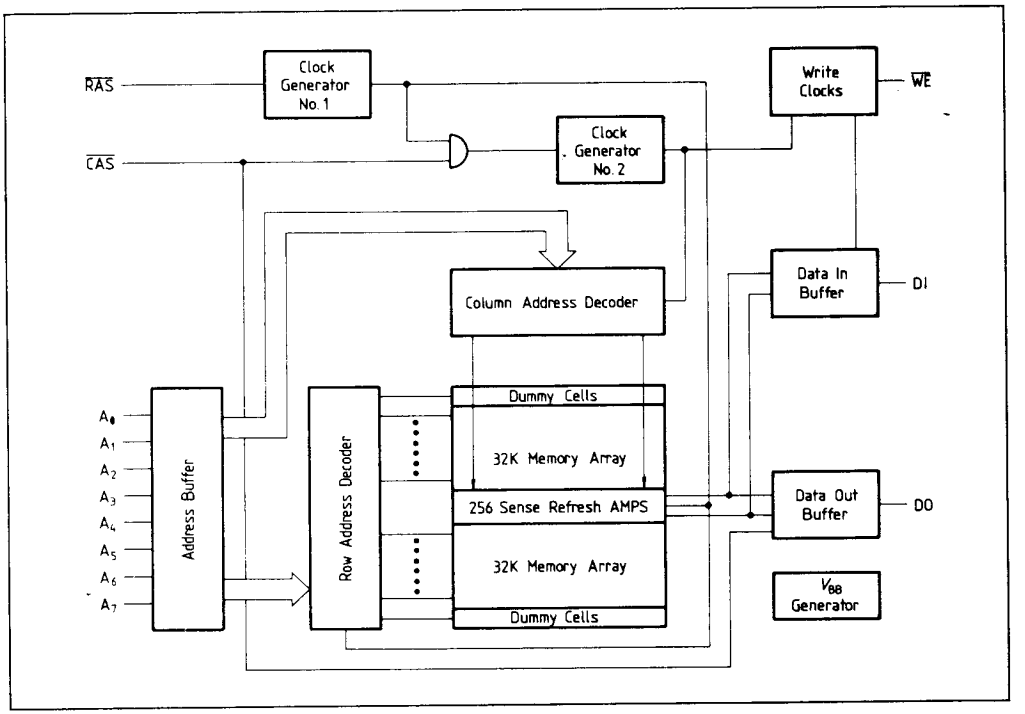
Block Diagram



Functional Description

Adressing (A_0–A_7)

For selecting one of the 65536 memory cells, a total of 16 address bits are required. First 8 row-address bits are set-up on pins A_0 trough A_7 and latched onto the row address latches by the Row Address Strobe ($\overline{RAS}$). Them the 8 column bits are set-up on pins A_0 through A_7 and latched onto the column address latches by the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or short after the falling edge of $\overline{RAS}$ and $\overline{CAS}$ respectively. $\overline{CAS}$ is internally gated by $\overline{RAS}$ to permit triggering of column address latches as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-address to column-address.
It should be noted that $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip-select activating the column decoder and the input and output buffers.

Write Enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (V_{IH}) on $\overline{WE}$ dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write of read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with set-up and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with set-up and hold times referenced to this signal.

Power On

An initial pause of 200 µs is required after power-up followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock sich as $\overline{RAS}$-only refresh) prior to normal operation. The current requirement of the HYB 4164 during power on is, however, dependent upon the input levels $\overline{RAS}$, $\overline{CAS}$ and the rise time of V_{CC}, as shown in the diagram following.

Data Output (DO)

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impecdance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (min) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). $\overline{CAS}$ going high returns the output to a high-impedance state. In an early write cycle the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

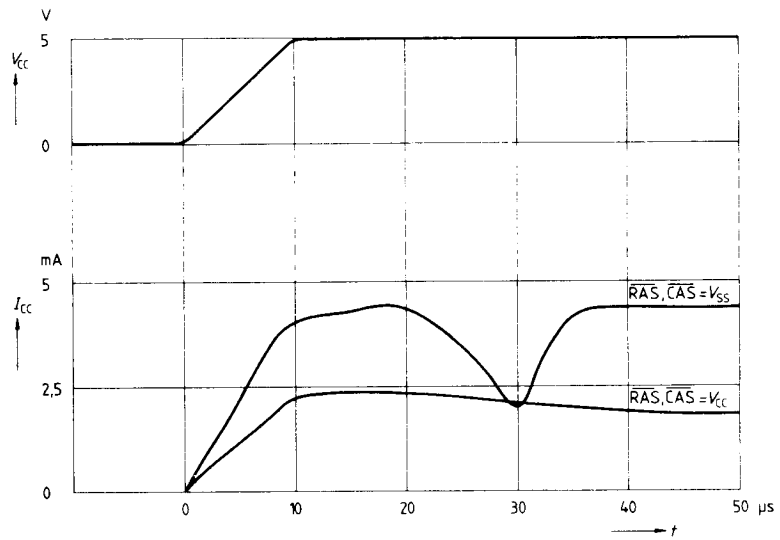
Hidden Refresh

$\overline{RAS}$ only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle.

Refresh Cycle

A refresh operation must be performed at least every four milli-seconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output signal during refresh. Strobing each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Current Consumption During Power up
(V_{CC} rise time 10 µs)



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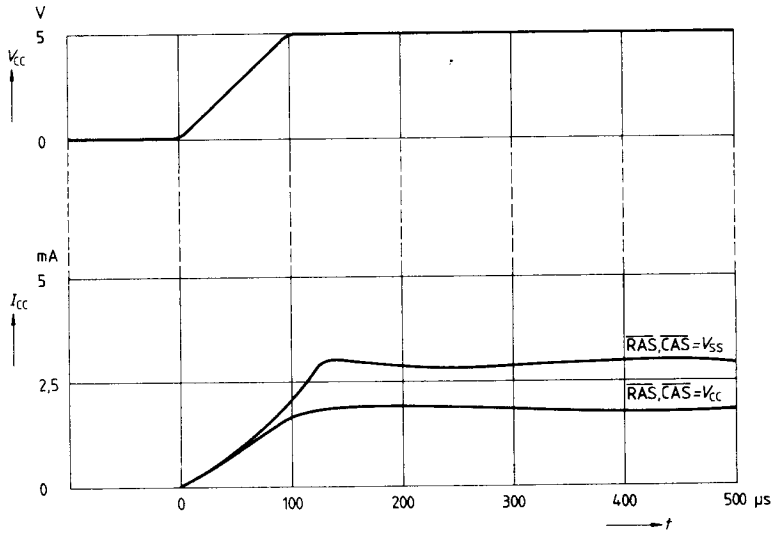
Current Consumption During Power up
(V_{CC} rise time 100 µs)



Absolute Maximum Ratings [1]

Operating Temperature Range	0 to + 70 °C
Storage Temperatures Range	−65 to +150 °C
Voltages on any Pin relative to V_{SS}	−1 to +7.0 V
Power Dissipation	1.0 W
Short Circuit Output Current	50 mA

A.C. Test Conditions

Input Pulse Levels		0.8 to 2.4 V
Input Rise and Fall Times	5 ns between	0.8 and 2.4 V
Input Timing Reference Levels		0.8 and 2.4 V
Output Timing Reference Levels		0.4 and 2.4 V
Output Load		Equivalent to 2 standard TTL Loads and 100 pF

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0 to 70 °C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions [1]
		Min.	Max.		
V_{IH}	High level input voltage (all inputs) [2]	2.4	6.0	V	–
V_{IL}	Low level input voltage [2]	−1.0	0.8		
V_{OH}	Output high voltage	2.4	V_{CC}		I_O = −5 mA
V_{OL}	Output low voltage	–	0.4		I_O = 4.2 mA
I_{CC1}	Average V_{CC} power supply current [3]	–	27	mA	–
I_{CC2}	Standby V_{CC} power supply current	–	3.5		$\overline{RAS}$ at V_{IH} $\overline{CAS}$ at V_{IH}
I_{CC3}	Average V_{CC} current during refresh [3]	–	24		$\overline{RAS}$ cycling $\overline{CAS}$ at V_{IH}
I_{CC4}	Page mode current [3]	–	20	mA	$\overline{RAS}$ at V_{IL} $\overline{CAS}$ cycling
$I_{I(L)}$	Input leakage current (any input) [4]	−10	10	µA	–
$I_{O(L)}$	Output leakage current	−10	10		$\overline{CAS}$ at V_{IH} V_O = V_{SS} to V_{CC}

Capacitances [5]

Symbol	Parameter [6]	Limit Values		Units	Test Conditions
		Min.	Max.		
C_{I1}	Input capacitance (A_0–A_7), DI	–	5	pF	–
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	–	10		–
C_O	Output capacitance	–	7		DO disabled

Notes:

1) An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.
2) Over- and undershooting on input levels of 6.5 V or −2 V for a period of 30 ns will not influence function and reliability of the device.
3) I_{CC} depends on frequency of operation, Maximum current is measured at 260 ns cycle rate.
4) AI device pins at 0 V and pin under test at +5.5 V.
5) Capacitance measured with a Boonton Meter 72 BD or effective capacitance calculated from the equation
$C = \frac{I \cdot \triangle t}{\triangle V}$ with $\triangle V$ = 3 V.
6) This parameter is periodically sampled and not 100% tested.

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A.C. Characteristics [1]

T_A = 0 to +70 °C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values						Units
		HYB 4164-1		HYB 4164-2		HYB 4164-3		
		Min.	Max.	Min.	Max.	Min.	max.	
t_{RC}	Random read or write cycle time [2]	220	–	280	–	330	–	ns
t_{RWC}	Read/write cycle time [2]	220	–	280	–	330	–	
t_{PC}	Page mode cycle time	125	–	170	–	225	–	
t_{RMWC}	Read/modify/write cycle time [2]	255	–	280	–	330	–	
t_{RAC}	Access time from $\overline{RAS}$ [3] [4]	–	120	–	150	–	200	
t_{CAC}	Access time from $\overline{CAS}$ [3] [5] [7]	–	80	–	100	–	135	
t_{OFF}	Output buffer turn-off delay [6]	–	35	–	40	–	50	
t_{RP}	$\overline{RAS}$ precharge time	90	–	100	–	120	–	
t_{RAS}	$\overline{RAS}$ pulse width	120	10^4	150	10^4	200	10^4	
t_{RSH}	$\overline{RAS}$ hold time	80	–	100	–	135	–	
t_{CSH}	$\overline{CAS}$ hold time	120	–	150	–	200	–	
t_{CAS}	$\overline{CAS}$ pulse width	80	–	100	–	135	–	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [7]	25	40	30	50	35	65	
t_{ASR}	Row address set-up time	0	–	0	–	0	–	
t_{RAH}	Row address hold time	15	–	20	–	25	–	
t_{ASC}	Column address set-up time	0	–	0	–	0	–	
t_{CAH}	Column address hold time	40	–	45	–	55	–	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	80	–	95	–	120	–	
t_{RCS}	Read command set-up time (RMW)	0	–	0	–	0	–	
t_{RCH}	Read command hold time	0	–	0	–	0	–	
t_{WCH}	Write command hold time	40	–	45	–	55	–	

Symbol	Parameter	Limit Values						Units
		HYB 4164-1		HYB 4164-2		HYB 4164-3		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95	–	110	–	120	–	ns
t_{WCS}	Write command set-up time [3]	−10	–	−10	–	−10	–	
t_{WP}	Write command pulse width	40	–	45	–	55	–	
t_{RWL}	Write command to $\overline{RAS}$ lead time	40	–	50	–	60	–	
t_{CWL}	Write command to $\overline{CAS}$ lead time	40	–	50	–	60	–	
t_{DS}	Data in set-up time	0	–	0	–	0	–	
t_{DH}	Data in hold time [9]	40	–	45	–	55	–	
t_{DHR}	Data in hold time [9] reference to $\overline{RAS}$	95	–	110	–	120	–	
t_{CP}	$\overline{CAS}$ precharge time (Page mode)	35	–	60	–	80	–	
t_{CPN}	$\overline{CAS}$ precharge time [10]	40	–	50	–	60	–	
t_{RF}	Refresh period	–	4.0	–	4.0	–	4.0	ms
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay [8]	60	–	60	–	80	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay [8]	110	–	120	–	145	–	
t_T	Transition time (Rise and Fall)	3	35	3	35	3	50	

Notes:

1) V_{IH} and V_{IL} are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

2) The specifications for $t_{RC(min)}$ and $t_{RWC(min)}$ are used only to indicate cycle time at which proper operation over full temperature range ($0\ °C \leq T_A \leq 70\ °C$) is assured.

3) Measured with a load equivalent to two standard TTL loads and 100 pF.

4) Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5) Assumes that $t_{RCD} \geq t_{RCD(max)}$.

6) $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7) Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{CWS(min)}$, the cycle is an early write cycle and the data-out will remain open circuit (high impedance) throughout the entire cycle: if $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ the cycles a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

9) t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write of read-modity-write cycles.

10) Not for page mode.

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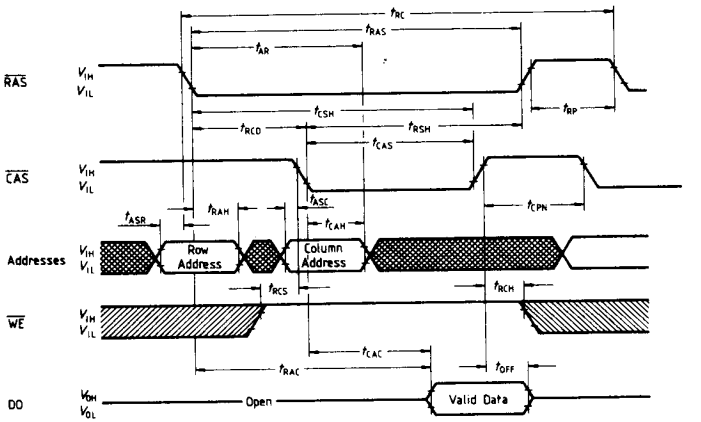
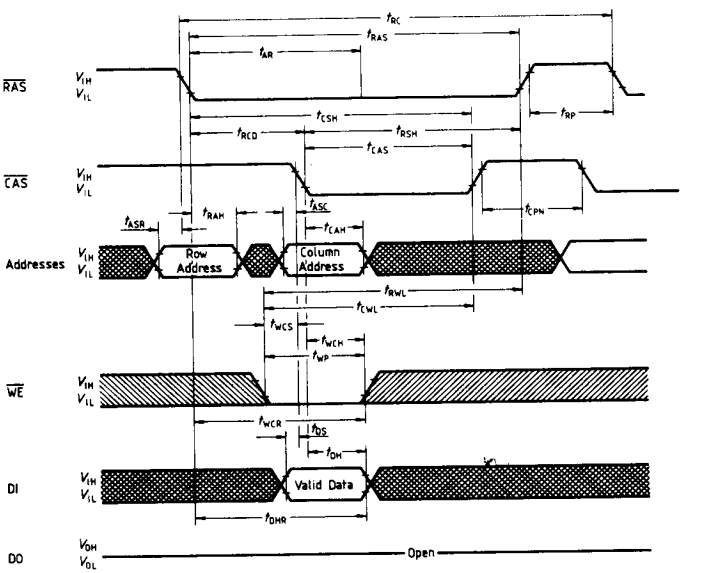
Waveforms

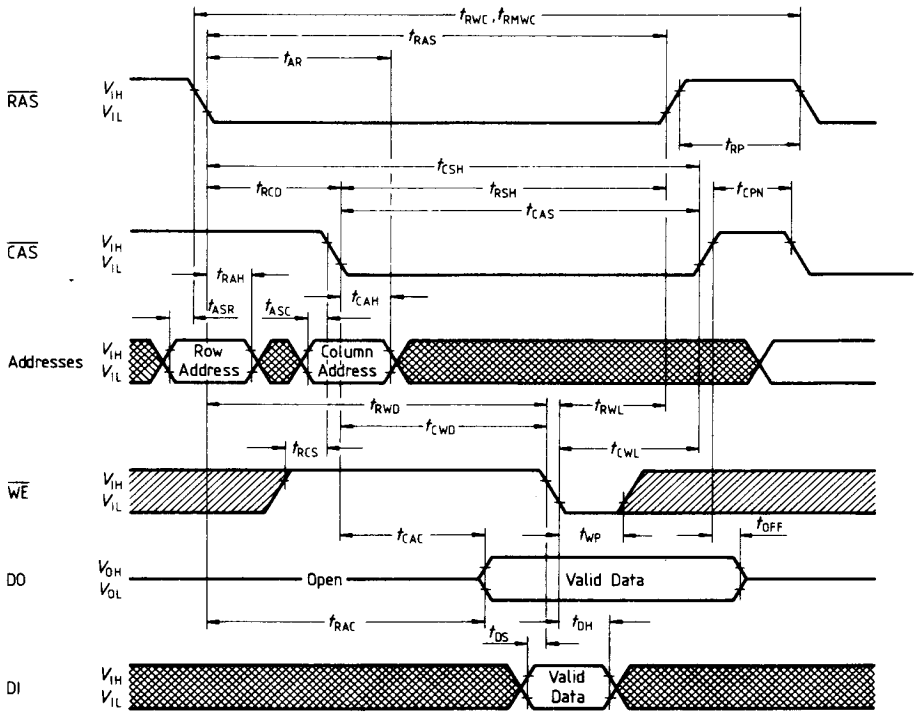
Read cycle



Write cycle (Early write)



Read-write/Read-modify-write cycle



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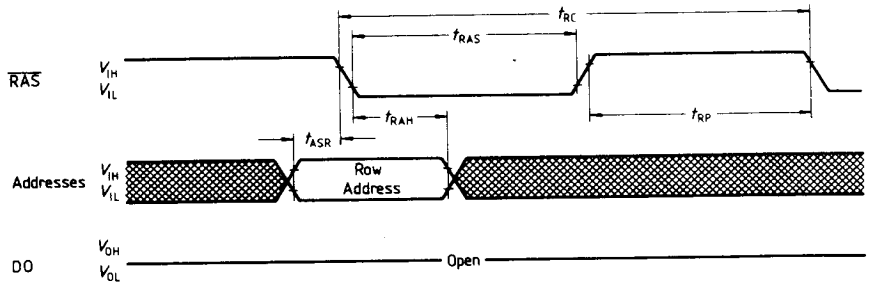
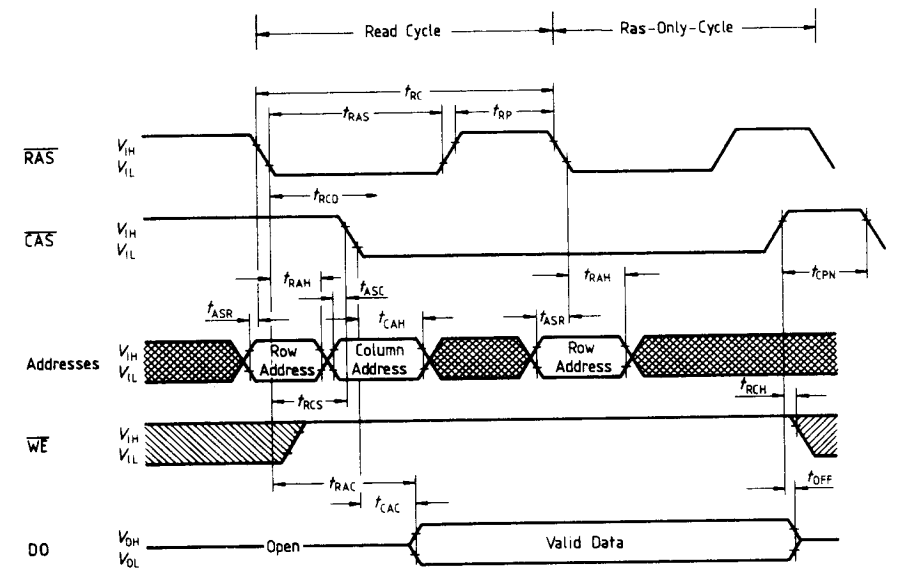
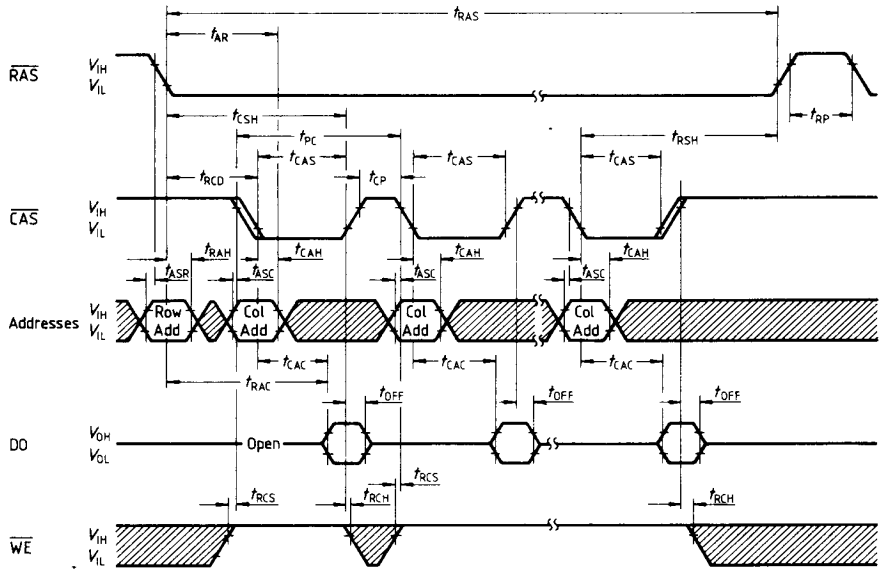
"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE
Note $\overline{\text{CAS}} = V_{IH}$; $\overline{\text{WE}}$ = Don't care



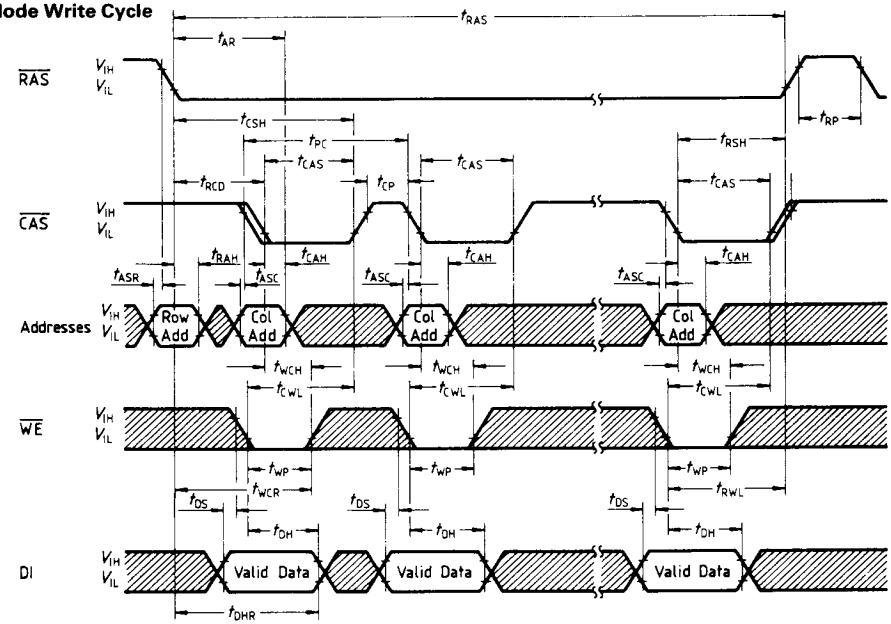
Hidden Refresh



Page Mode Read Cycle

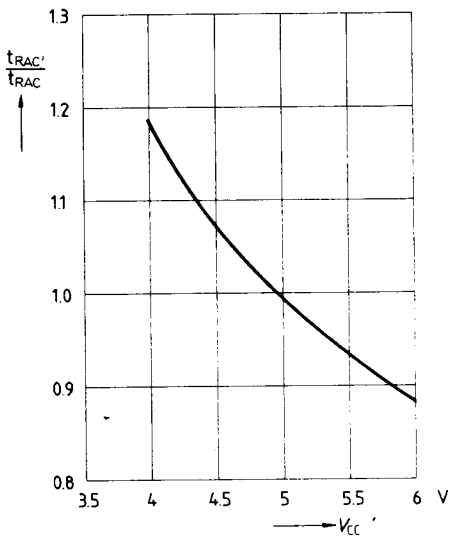


Page Mode Write Cycle

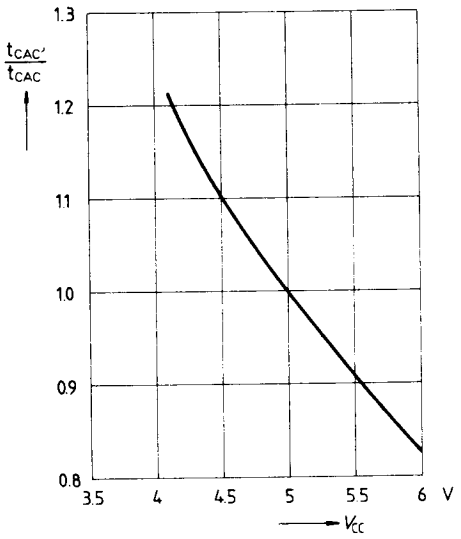


Typical Access Time Curves

$\overline{RAS}$ Access Time vs. Supply Voltage
$T_A = 25\,°C$

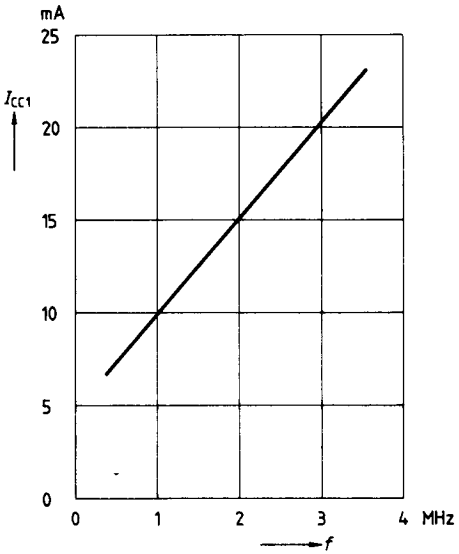


$\overline{CAS}$ Access Time vs. Supply Voltage
$T_A = 25\,°C$

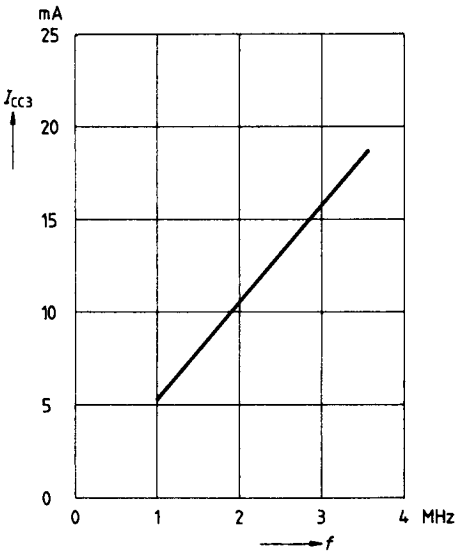


Typical Current Consumption Curves

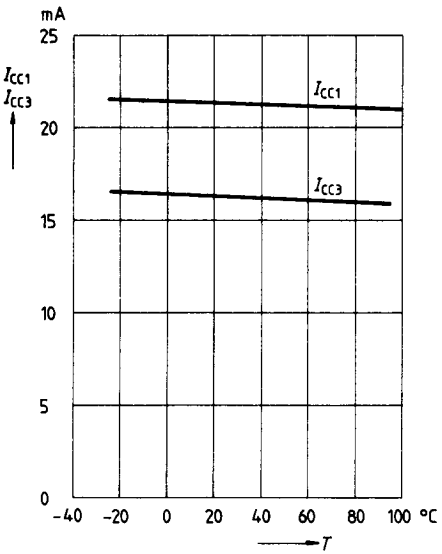
I_{CC1} **(Average) vs. Cycle Rate**
V_{CC} **= 5.5 V**
Write Cycle
T_A = 25 °C



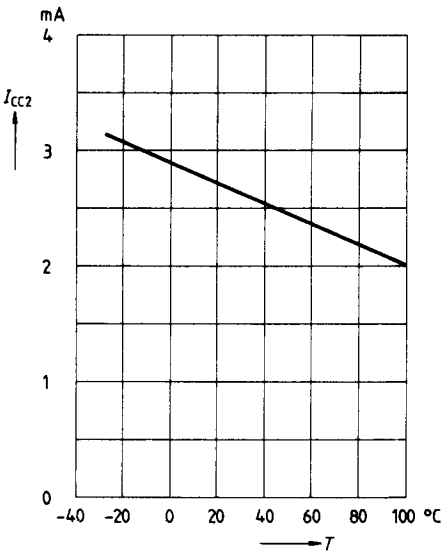
I_{CC3} **(Average) vs. Cycle Rate**
V_{CC} **= 5.5 V**
RAS Only Refresh Cycle
T_A = 25 °C



I_{CC} **(Average) vs. Temperature (typ.)**
V_{CC} **= 5.5 V,** t_{RC} **= 280 nsec**
I_{CC1} **Write cycle**
I_{CC3} **RAS Only Refresh Cycle**



I_{CC2} **Standby current vs. temperature (typ.)**
V_{CC} **= 5.5 V**



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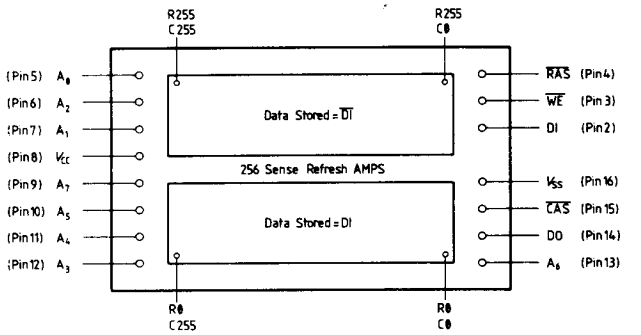
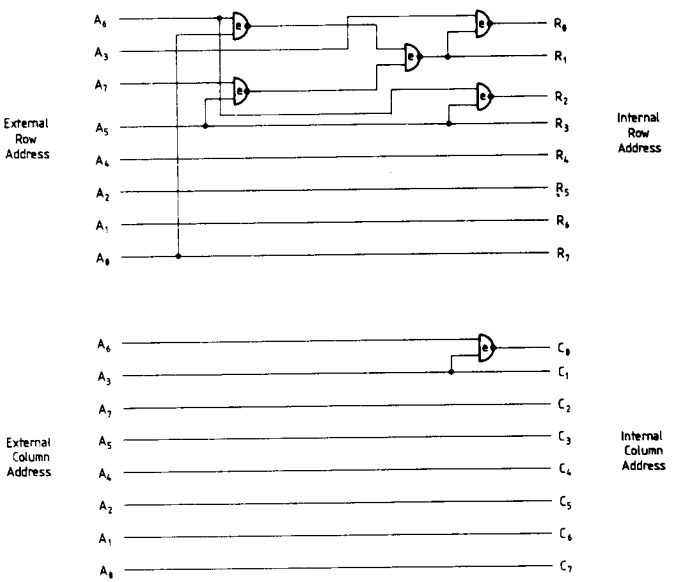
Topology Description

The evaluation and incoming testing of RAMs normally requires a description of the internal topology of the device in order to check for "worst case" pattern.

Internal Topology



Address Decoder scrambling



Internal Data Polarity
Data Stored = DI ⊕ $A_{0\,(ROW)}$

Note:
The logic symbol "exclusiv nor" is used solely to indicate the logic function

Ordering Information

Type	Description
HYB4164-P1	RAM, 120 ns (P-DIP 16)
HYB4164-P2	RAM, 150 ns (P-DIP 16)
HYB4164-P3	RAM, 200 ns (P-DIP 16)