

LM66200 1.6 V to 5 V, 2.5-A Dual Ideal Diode With Automatic Switchover

1 Features

- Input voltage range: 1.6 V to 5.5 V
- Maximum continuous current: 2.5 A
- On-resistance: 40 mΩ (typical)
- Standby current: 50 nA (typical)
- Quiescent current: 1.32 μA (typical)
- Automatic diode switchover
- Controlled output slew rate:
 - 1.3 ms (typical) at 3.3 V
- Reverse current blocking when VOUT > VINx
- Thermal shutdown

2 Applications

- Electricity meters
- Motor drives
- Building automation
- Electronic point of sale
- Asset tracker

3 Description

The LM66200 is a dual ideal diode device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 2.5 A per channel. The device uses N-channel MOSFETs to switch between supplies while providing a controlled slew rate when voltage is first applied.

Due to its low quiescent of 1.32 μA (typical) and low standby current of 50 nA (typical), the LM66200 is ideal for systems where a battery is connected to one of the inputs. These low currents extend the life and operation of the battery when in use.

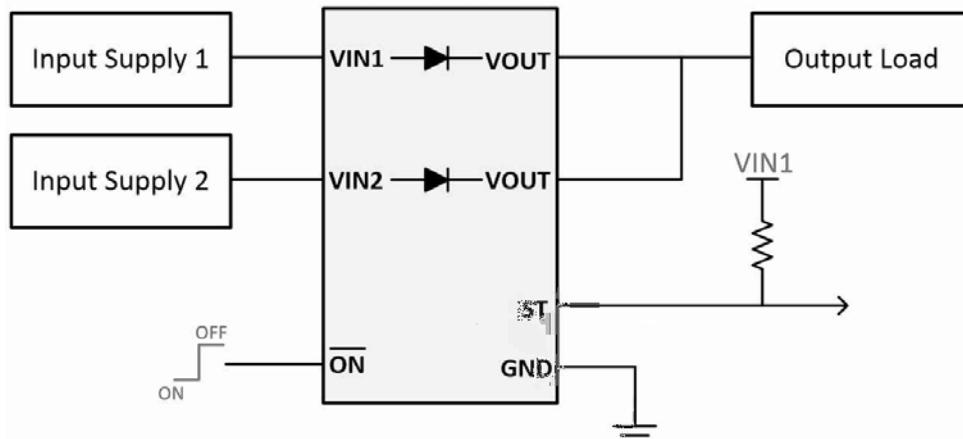
The LM66200 uses automatic diode mode to prioritize the highest voltage supply and pass it through to the output. The active low enable pin (ON) disables both channels, allowing the user to put the device into shutdown mode when neither supply is needed.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM66200	SOT (8)	2.1 mm × 1.6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

LM66200



Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features	1	7.5 Output Voltage Drop.....	10
2 Applications	1	7.6 Device Functional Modes.....	10
3 Description	1	8 Application and Implementation	11
4 Revision History	2	8.1 Application Information.....	11
5 Pin Configuration and Functions	3	8.2 Typical Application.....	11
6 Specifications	4	9 Power Supply Recommendations	13
6.1 Absolute Maximum Ratings.....	4	10 Layout.....	13
6.2 ESD Ratings.....	4	10.1 Layout Guidelines.....	13
6.3 Recommended Operating Conditions.....	4	10.2 Layout Example.....	13
6.4 Thermal Information.....	4	11 Device and Documentation Support	14
6.5 Electrical Characteristics.....	5	11.1 Documentation Support.....	14
6.6 Switching Characteristics.....	6	11.2 Receiving Notification of Documentation Updates.....	14
6.7 Typical Characteristics.....	7	11.3 Trademarks.....	14
7 Detailed Description	9	11.4 Electrostatic Discharge Caution.....	14
7.1 Overview.....	9	11.5 Glossary.....	14
7.2 Functional Block Diagram.....	9	12 Mechanical, Packaging, and Orderable	
7.3 Feature Description.....	9	Information	14
7.4 VINx Collapse Rate.....	10		

4 Revision History

DATE	REVISION	NOTES
November 2021	*	Initial release.

5 Pin Configuration and Functions

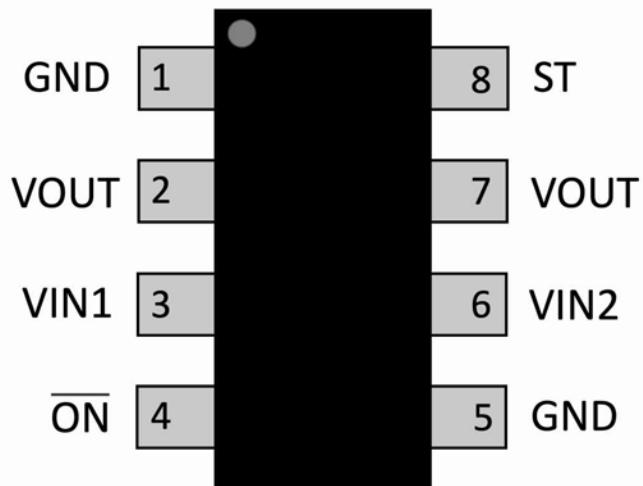


Figure 5-1. DRL Package 8-Pin SOT Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1, 5	—	Device ground
VOUT	2, 7	O	Output power
VIN1	3	I	Channel 1 input power
ON	4	I	Active low enable pin. Device is enabled when ON is pulled low and the device turns off both channels when ON is pulled high.
VIN2	6	I	Channel 2 input power
ST	8	O	Status pin. Pulled high when VIN1 is being used and pulled low when VIN2 is being used. Can be pulled up to VIN1 to reduce quiescent current when VIN2 is powering the output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{IN1}, V_{IN2}	Input Voltage	-0.3	6	V
V_{OUT}	Output Voltage	-0.3	6	V
V_{ST}, V_{ON}	Control Pin Voltage	-0.3	6	V
I_{MAX}	Maximum Current		2.5	A
$I_{MAX,PLS}$	Maximum Pulsed Current Max duration 1ms, Duty cycle of 2%		4	A
T_J	Junction temperature	Internally Limited		°C
T_{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN1}, V_{IN2}	Input Voltage	1.6	5.5	5.5	V
V_{OUT}	Output Voltage	0	5.5	5.5	V
V_{ST}, V_{ON}	Control Pin Voltage	0	5.5	5.5	V
T_A	Ambient Temperature	-40	125	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM66200	UNIT
		DRL (SOT)	
		8-PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.5	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	19.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.1	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
Power Consumption							
I _{STBY, VIN1}	VIN1 Standby Current	VIN2 powers V _{OUT} VIN2 > VIN1 + 0.2 V	25°C	0.22			uA
			-40°C to 85°C		0.31		uA
			-40°C to 105°C		0.32		uA
I _{STBY, VIN2}	VIN2 Standby Current	VIN1 powers V _{OUT} VIN1 > VIN2 + 0.1 V	25°C	0.05			uA
			-40°C to 85°C		0.07		uA
			-40°C to 105°C		0.09		uA
I _{Q, VIN1}	VIN1 Quiescent Current	VIN1 powers V _{OUT} VIN1 > VIN2 + 0.1 V	25°C	1.32			uA
			-40°C to 85°C		3.6		uA
			-40°C to 105°C		4.4		uA
I _{Q, VIN2}	VIN2 Quiescent Current	VIN2 powers V _{OUT} VIN2 > VIN1 + 0.2 V	25°C	1.35			uA
			-40°C to 85°C		3.7		uA
			-40°C to 105°C		4.5		uA
I _{SD, VIN1}	VIN1 Shutdown Current	ON = 5 V VIN1 > VIN2 V _{OUT} = 0 V	25°C	0.1			uA
			-40°C to 85°C		1.3		uA
			-40°C to 105°C		2.9		uA
		ON = 5 V VIN1 < VIN2 V _{OUT} = 0 V	25°C	0.05			uA
			-40°C to 85°C		1		uA
			-40°C to 105°C		2.4		uA
I _{SD, VIN2}	VIN2 Shutdown Current	ON = 5 V VIN2 > VIN1 V _{OUT} = 0 V	25°C	0.05			uA
			-40°C to 85°C		1.3		uA
			-40°C to 105°C		2.9		uA
		ON = 5 V VIN2 < VIN1 V _{OUT} = 0 V	25°C	0.05			uA
			-40°C to 85°C		0.7		uA
			-40°C to 105°C		2.1		uA
I _{ON}	ON pin leakage	VIN1 = VIN2 = PR1 = 5.5 V	-40°C to 105°C		0.1		uA
I _{ST}	ST pin leakage	VIN1 = VIN2 = ST = 5.5 V	-40°C to 105°C		0.03		uA
Performance							
R _{ON}	On-Resistance	VIN _x = 5 V I _{OUT} = 200 mA	25°C	37	46		mΩ
			-40°C to 85°C		55		mΩ
			-40°C to 105°C		60		mΩ
		VIN _x = 3.3 V I _{OUT} = 200 mA	25°C	40	48		mΩ
			-40°C to 85°C		55		mΩ
			-40°C to 105°C		59		mΩ
		VIN _x = 1.8 V I _{OUT} = 200 mA	25°C	41	51		mΩ
			-40°C to 85°C		61		mΩ
			-40°C to 105°C		66		mΩ
		VIN _x = 1.6 V I _{OUT} = 200 mA	25°C	42	52		mΩ
			-40°C to 85°C		68		mΩ
			-40°C to 105°C		74		mΩ
V _{OL,ST}	Status pin V _{OL}	I _{ST} = 1 mA	-40°C to 105°C		0.1		V
t _{ST}	Status pin response time		-40°C to 105°C		5		us
V _{ON}	ON reference voltage	1.6 V ≤ VIN _x ≤ 5.5 V	-40°C to 105°C	0.8	1	1.2	V
Protection							

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

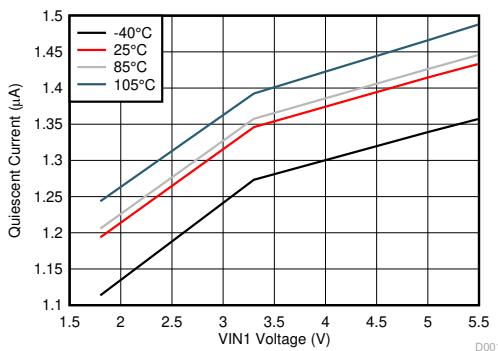
PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{RCB}	Reverse current blocking response time V _{OUT} > V _{INx} + 1 V	-40°C to 105°C		2		us
V _{RCB,R}	Reverse current blocking rising threshold 1.6 V ≤ V _{INx} ≤ 5.5 V	-40°C to 105°C		42	70	mV
V _{RCB,F}	Reverse current blocking falling threshold 1.6 V ≤ V _{INx} ≤ 5.5 V	-40°C to 105°C		17	40	mV
I _{RCB}	Reverse current blocking activation current 1.6 V ≤ V _{INx} ≤ 5.5 V	-40°C to 105°C		1.4	4	A
TSD	Thermal shutdown	-		170		°C
TSD _{HYS}	Thermal shutdown hysteresis	-		20		°C

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

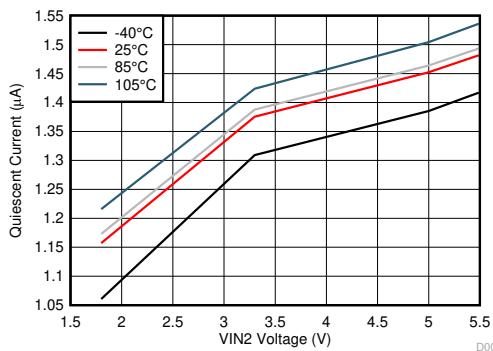
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switchover					
t _{sw}	Switchover time, V _{INx} = 5 V R _L = 10Ω, C _L = 10uF		8		us
t _{sw}	Switchover time, V _{INx} = 3.3 V R _L = 10Ω, C _L = 10uF		6.2		us
t _{sw}	Switchover time, V _{INx} = 1.8 V R _L = 10Ω, C _L = 10uF		17.7		us
t _D	Delay time, V _{INx} = 5 V R _L = 100Ω, C _L = 10uF		1		ms
t _D	Delay time, V _{INx} = 3.3 V R _L = 100Ω, C _L = 10uF		1.2		ms
t _D	Delay time, V _{INx} = 1.8 V R _L = 100Ω, C _L = 10uF		1.4		ms
t _{ss}	Soft-start time, V _{INx} = 5 V R _L = 100Ω, C _L = 10uF		1.7		ms
t _{ss}	Soft-start time, V _{INx} = 3.3 V R _L = 100Ω, C _L = 10uF		1.3		ms
t _{ss}	Soft-start time, V _{INx} = 1.8 V R _L = 100Ω, C _L = 10uF		0.9		ms

6.7 Typical Characteristics



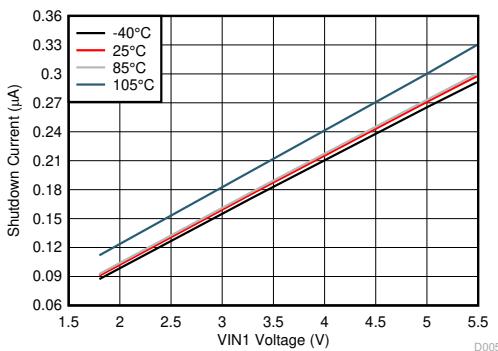
VIN2 = 1.6 V VOUT = Open

Figure 6-1. VIN1 Quiescent Current vs Input Voltage



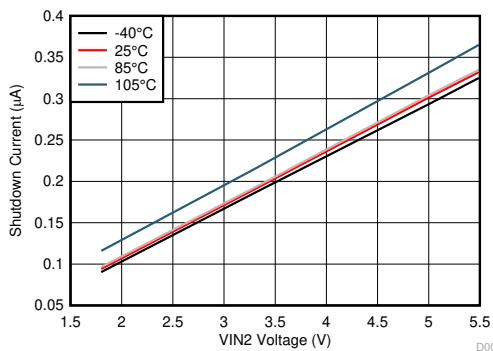
VIN1 = 1.6 V VOUT = Open

Figure 6-2. VIN2 Quiescent Current vs Input Voltage



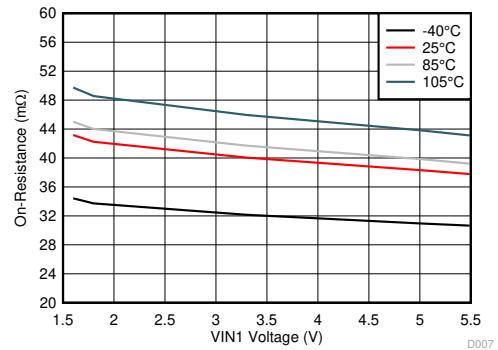
VIN2 = 1.6 V VOUT = 0 V

Figure 6-3. VIN1 Shutdown Current vs Input Voltage



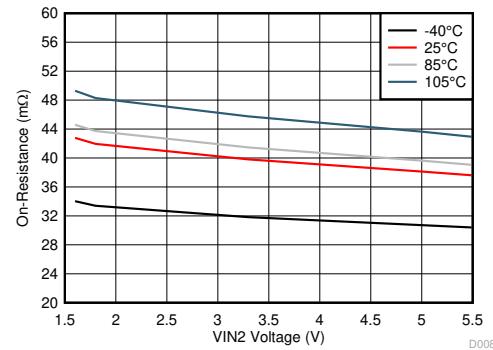
VIN1 = 1.6 V VOUT = 0 V

Figure 6-4. VIN2 Shutdown Current vs Input Voltage



I_{OUT} = 200 mA

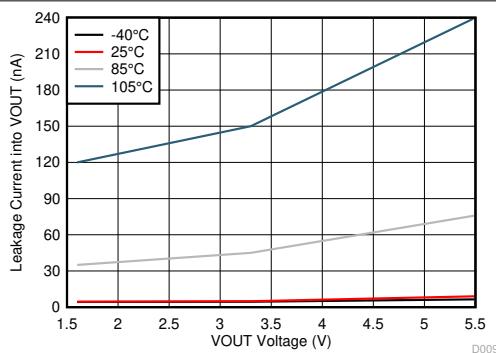
Figure 6-5. Channel 1 On-Resistance vs Input Voltage



I_{OUT} = 200 mA

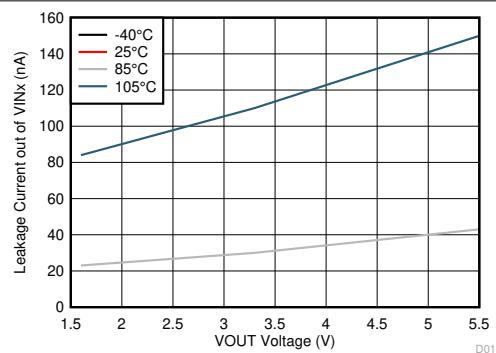
Figure 6-6. Channel 2 On-Resistance vs Input Voltage

6.7 Typical Characteristics (continued)



V_{INx} = 0 V V_{INy} = Open

Figure 6-7. Reverse Leakage Current into VOUT



V_{INx} = 0 V V_{INy} = Open

Figure 6-8. Reverse Leakage Current out of VINx

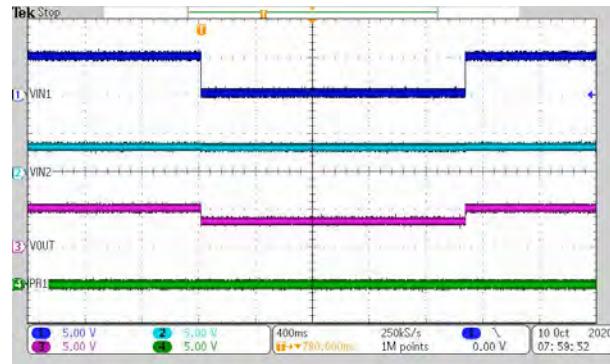


Figure 6-9. Diode Mode Switchover Behavior (R_L = 10 Ω, CL = 10 μF)

7 Detailed Description

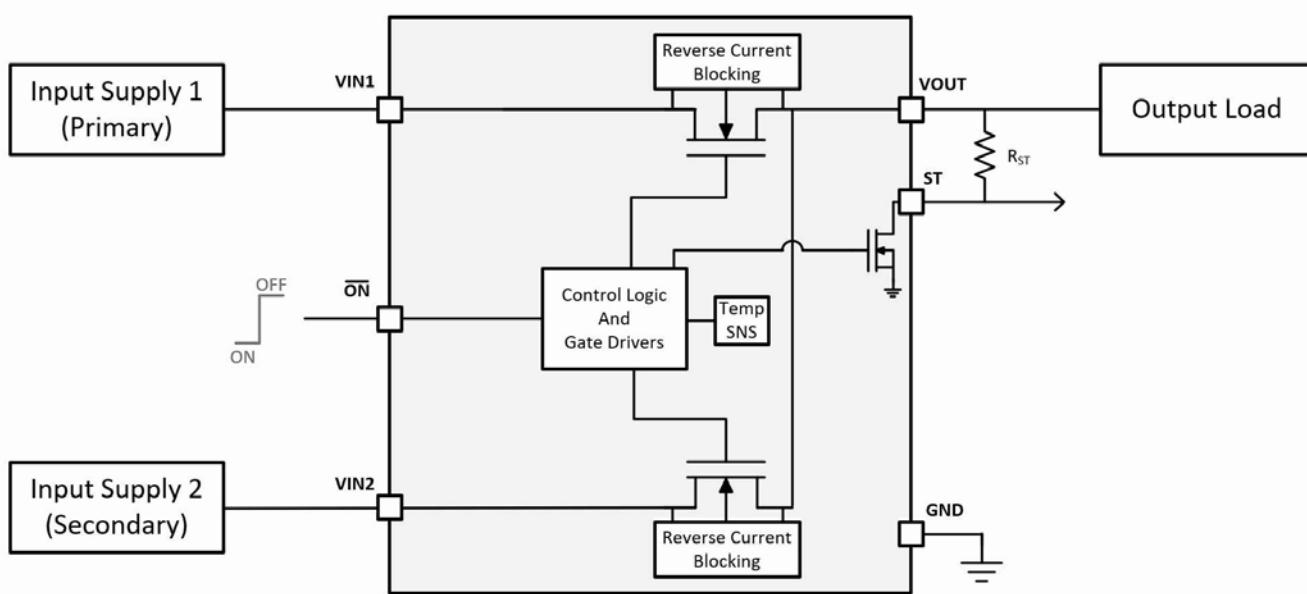
7.1 Overview

The LM66200 is a dual ideal diode device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 2.5 A per channel. The device uses N-channel MOSFETs to switch between supplies, while providing a controlled slew rate when voltage is first applied.

When in operation, the device has a quiescent of 1.32 μ A (typical), which is drawn from the highest VINx supply. The lower voltage VINx supply only sees a standby current of 50 nA (typical).

The LM66200 uses automatic diode mode to prioritize the highest voltage supply and pass it through to the output. The active low enable pin (\overline{ON}) allows the user to disable both channels, putting the device into shutdown mode when neither supply is needed.

7.2 Functional Block Diagram



7.3 Feature Description

The below sections detail the features of the LM66200.

7.3.1 Truth Table

The below table shows the expected behavior of the LM66200.

VIN1	VIN2	ON	ST	VOUT
VIN1 > VIN2		Low	High	VIN1
VIN1 < VIN2		Low	Low	VIN2
X	X	High	Low	Hi-Z

X = do not care

7.3.2 Soft Start

When an input voltage is applied to the LM66200 and the output voltage is lower than 1 V, the output is brought up with soft start to minimize the inrush current due to output capacitance. During switchover, soft start is not used to minimize output voltage drop. For linear soft start behavior, iTI recommends to have an output capacitance of at least 0.1 μ F.

7.3.3 Status Indication

The ST pin is an open drain output that must be pulled up to an external voltage for proper operation. When the LM66200 is powering the output using VIN1, the ST pin is pulled high. When the LM66200 is powering the output using VIN2, the ST pin is pulled low. During a fault condition the ST pin is pulled low, regardless of the channel being used.

7.4 VINx Collapse Rate

The LM66200 uses the highest voltage supply to power the device. When one supply drops below the other, the device changes the supply used to power the device. If the supply powering the device drops at a rate faster than $1\text{ V}/10\text{ }\mu\text{s}$, the other supply must be at 2.5 V or higher to prevent the device from resetting. If the other supply is lower than 2.5 V, then the device is not be able to switch to the supply quickly enough, and the device resets and turns on with soft start timing. To slow down the decay of the input, capacitance can be added to the input or output.

7.5 Output Voltage Drop

The output voltage drop is based on the load capacitance and load resistance. The stronger the resistive load, the faster the output discharges during switchover. The higher the capacitance on the output, the less the voltage drops during switchover.

7.6 Device Functional Modes

The below sections detail the operation of the LM66200 device.

7.6.1 Automatic Switchover

When both inputs are applied to the device, the highest voltage is used to power the output. If the $\overline{\text{ON}}$ pin is used as an active low device enable, turning off the device when it is pulled high. When the device is turned back on, soft start is used to power the output. The expected behavior for the device is shown in the waveform below.

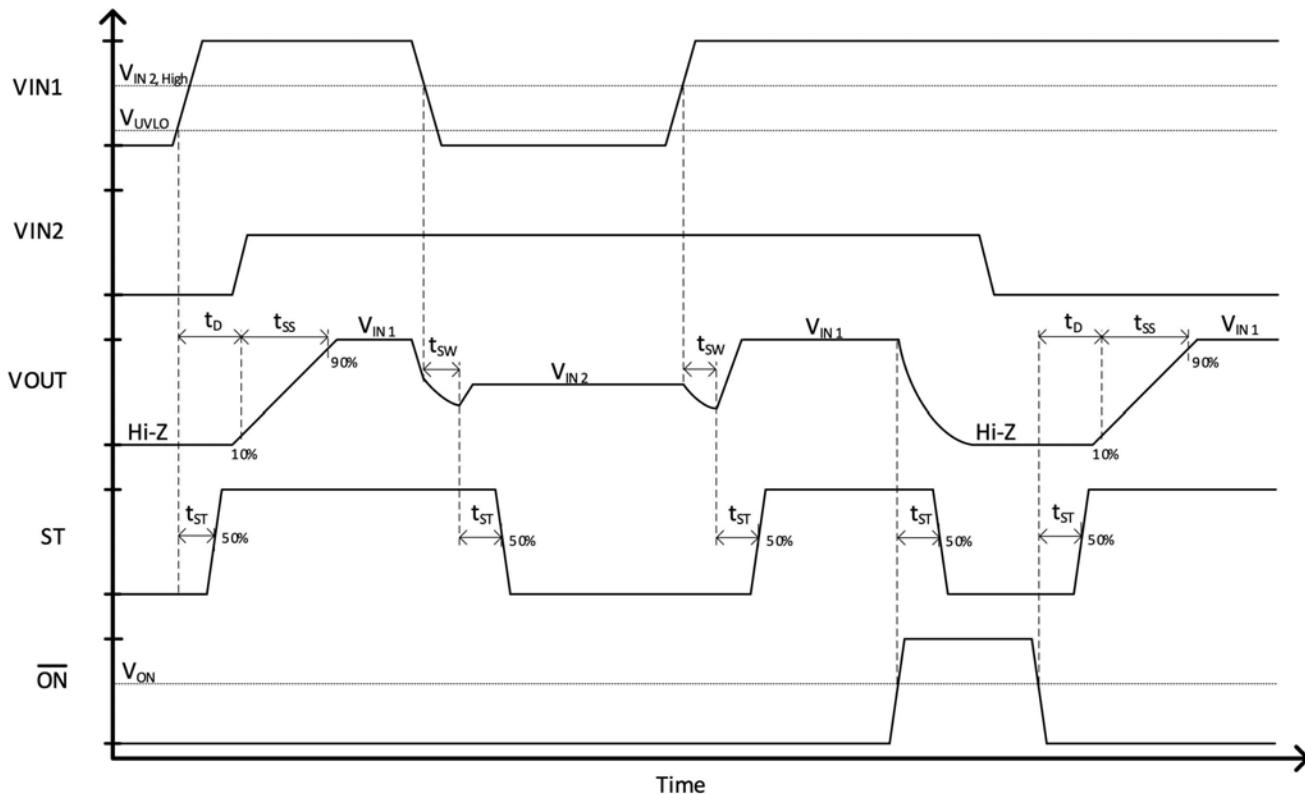


Figure 7-1. Automatic Switchover Waveform

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

8.2 Typical Application

This typical application demonstrates how the LM66200 device can be used to control inrush current for high output capacitances.

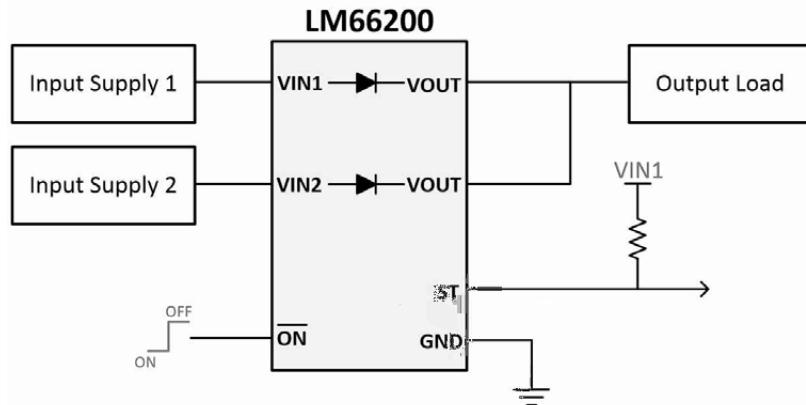


Figure 8-1. LM66200 Typical Application Diagram

8.2.1 Design Requirements

For this example, the values below are used as the design parameters.

Table 8-1. Design Parameters

PARAMETER	VALUE
VIN1 input voltage	5 V
Output capacitance	100 μ F
Maximum inrush current	500 mA

8.2.2 Detailed Design Procedure

Use [Equation 1](#) to determine how much inrush current is caused by the output capacitor.

$$I_{\text{INRUSH}} = C_{\text{OUT}} \times V_{\text{OUT}} / t_{\text{ss}} \quad (1)$$

where

- I_{INRUSH} = amount of inrush current caused by C_{OUT}
- C_{OUT} = capacitance on V_{OUT}
- t_{ss} = output voltage soft start time
- V_{OUT} = final value of the output voltage

With a final output voltage of 5 V, the expected rise time is 1.7 ms. Using the inrush current equation, the inrush current caused by a 100- μF capacitance is 294 mA, well below the 500-mA target.

8.2.3 Application Performance Plots

The below oscilloscope capture shows 5 V being applied to V_{IN1} . The output comes up with slew rate control and limits the inrush current to below 500 mA.

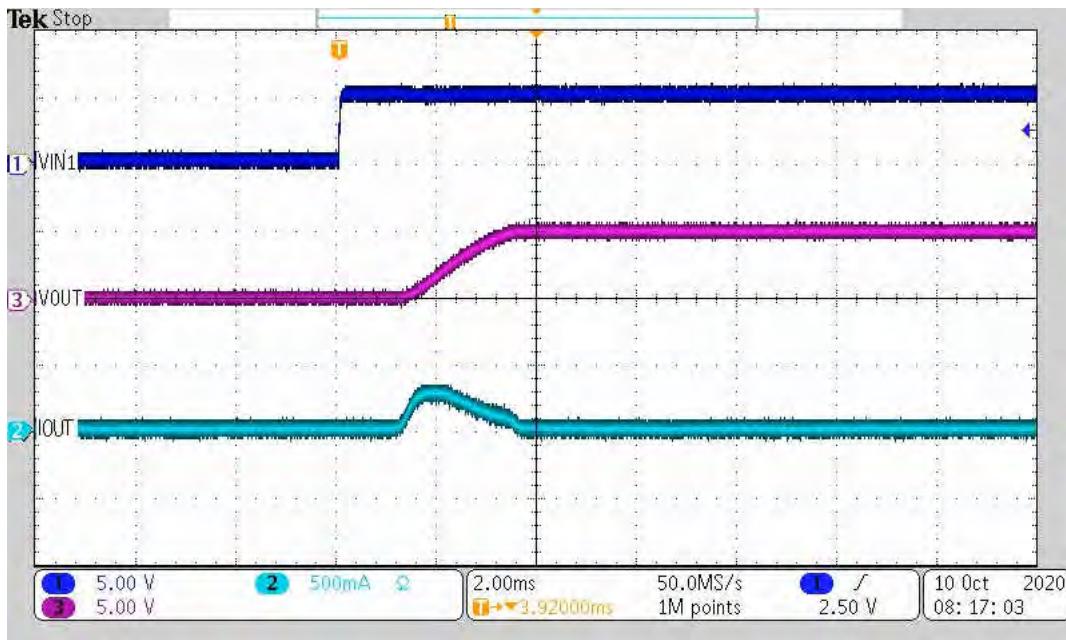


Figure 8-2. LM66200 Inrush Current Control

9 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supplies must be well regulated and placed as close to the device terminals as possible. The power supplies must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 μ F is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

10 Layout

10.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN1, VIN2, VOUT, and GND helps minimize the parasitic electrical effects.

10.2 Layout Example

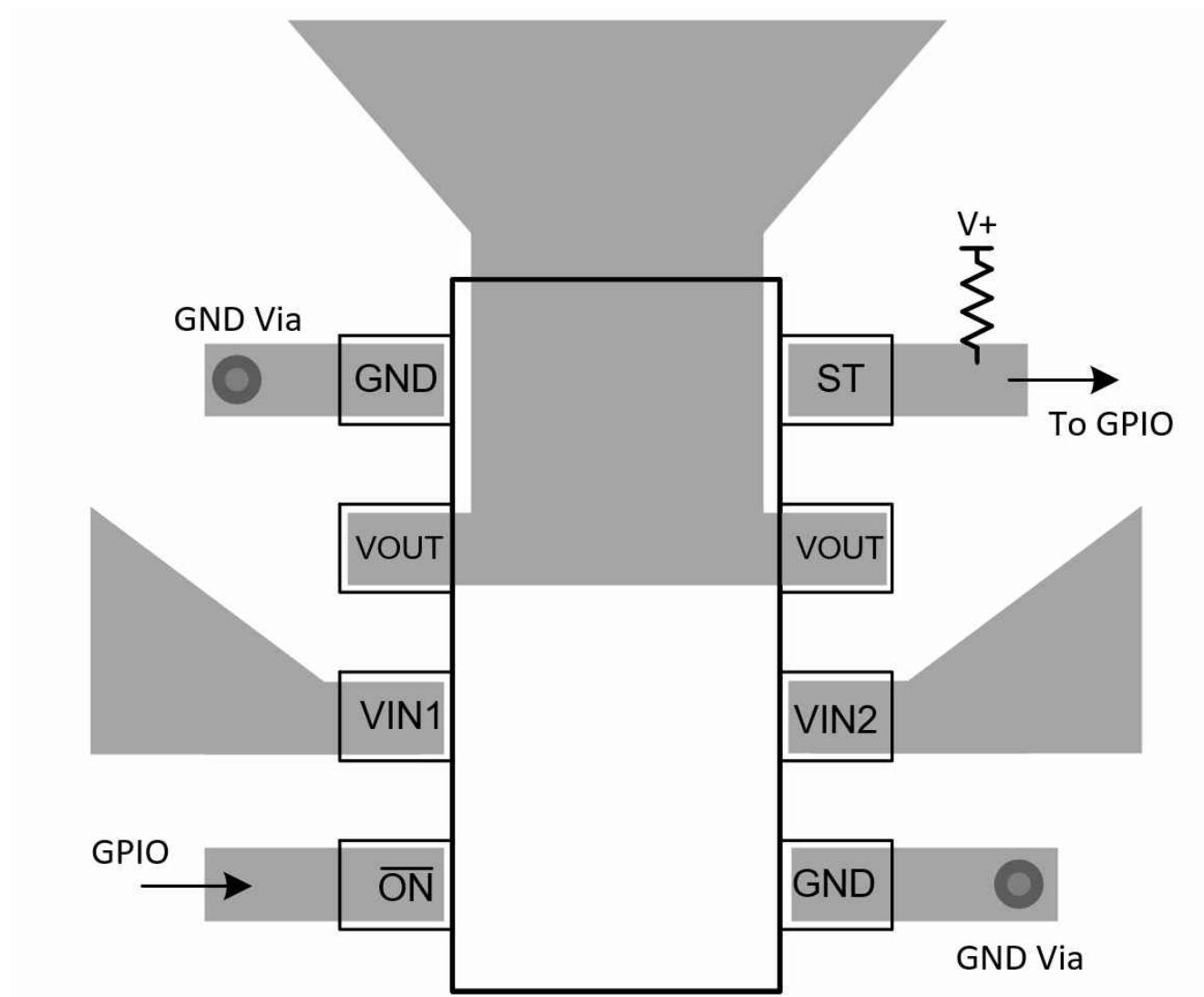


Figure 10-1. LM66200 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Basics of Power MUX](#) application note
- Texas Instruments, [11 Ways to Protect Your Power Path](#) e-book

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM66200DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	LM66	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

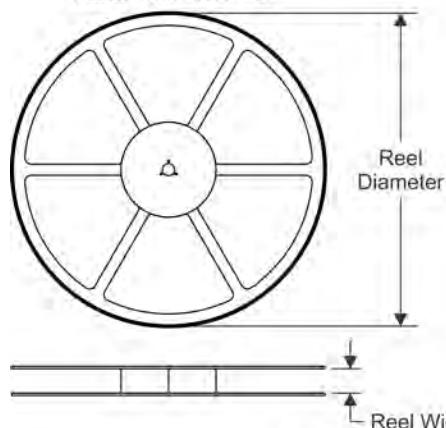
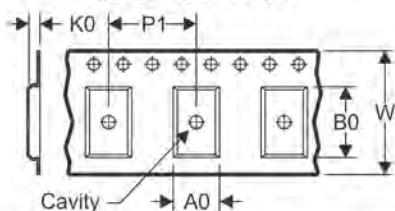
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

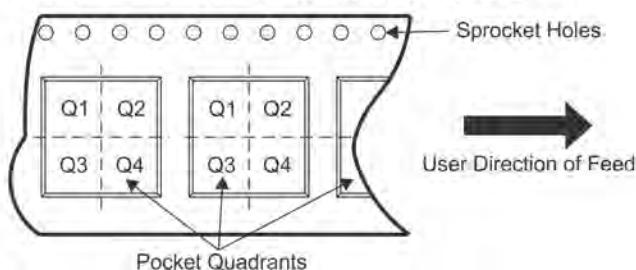
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM66200DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

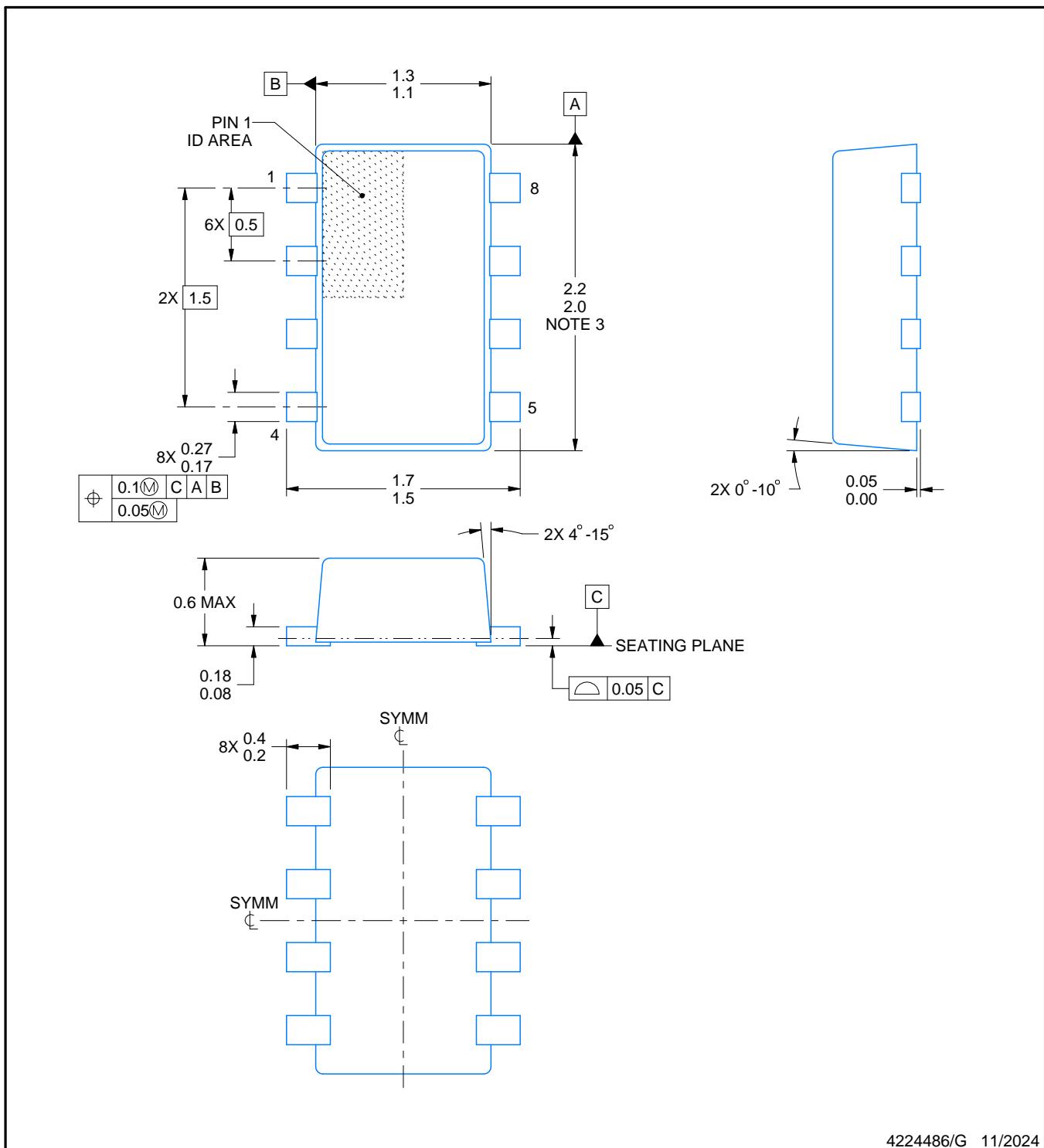
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM66200DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/G 11/2024

NOTES:

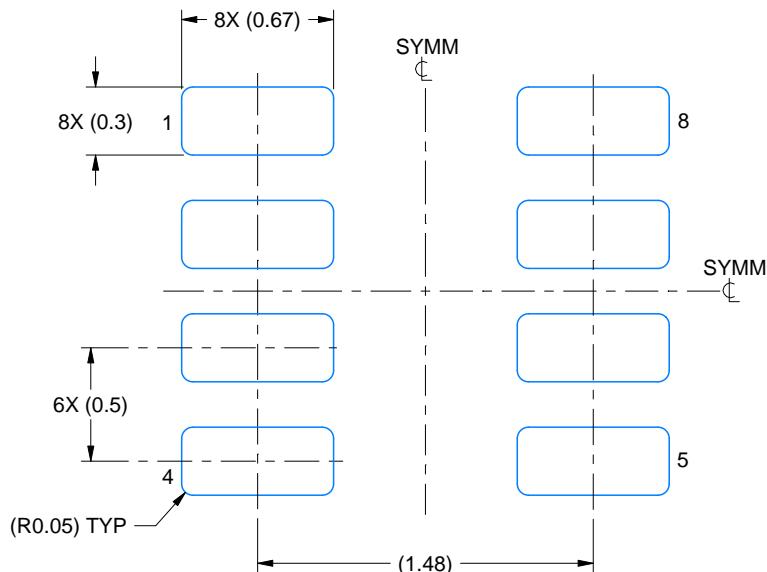
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

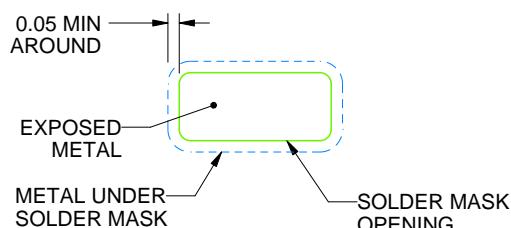
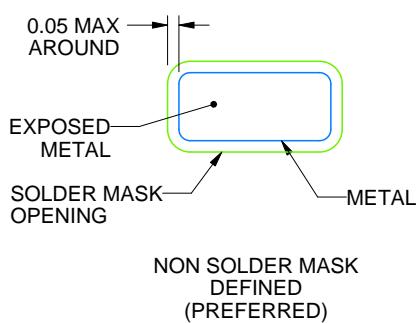
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

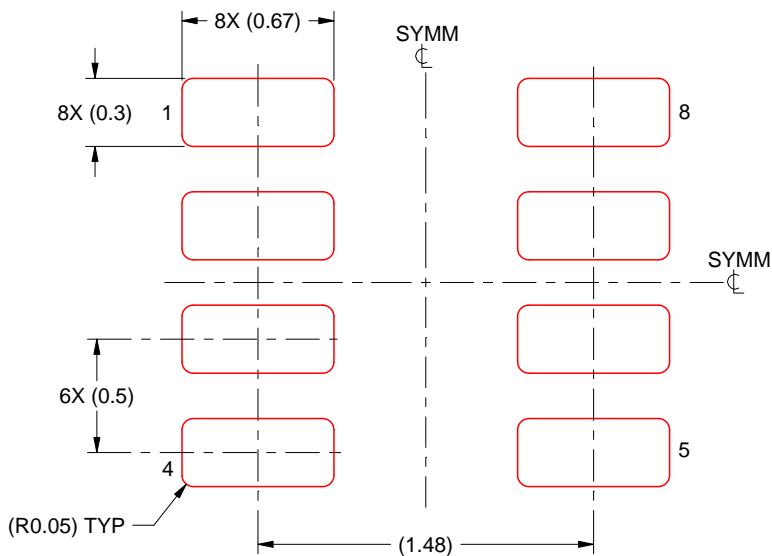
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated