Signetics

FAST 74F151, 74F151A
Multiplexers

FAST Products

74F151 8-Input Multiplexer
74F151A 8-Input Multiplexer
Product Specification

FEATURES

- **High speed 8-to-1 multiplexing**
- **On chip decoding**
- **Multifunction capability**
- **Complementary outputs**
- **See 'F251/'F251A for 3-state version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151	5.5ns	13.5mA
74F151A	4.5ns	17mA

DESCRIPTION

The 74F151 and 74F151A are logic implementations of a single-pole, 8- position switch with the switch position controlled by the state of three Select (S_0, S_1, S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High, the $\overline{Y}$ output is High and the Y output is Low, regardless of all other inputs. In one package the 74F151 or 74F151A provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and the negation with correct manipulation.

74F151A is the faster version of 74F151.

ORDERING INFORMATION

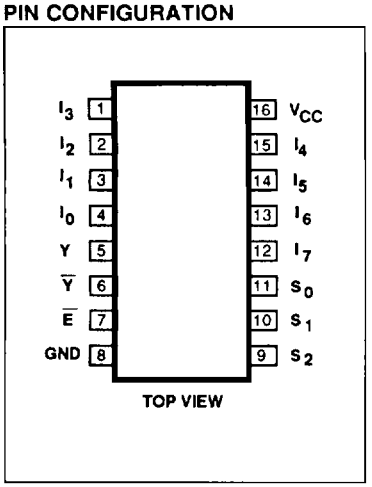
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F151N, N74F151AN
16-Pin Plastic SO	N74F151D, N74F151AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0- I_7	Data inputs	1.0/1.0	20µA/0.6mA
S_0- S_2	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y, $\overline{Y}$	Data outputs	150/33	3mA/20mA

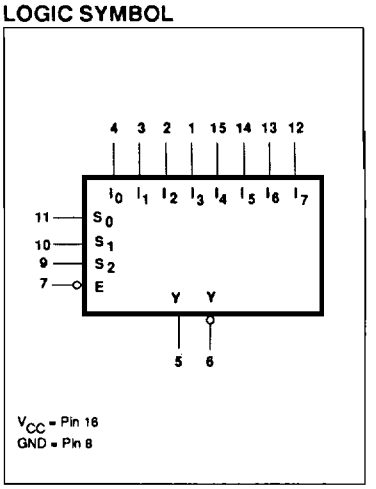
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

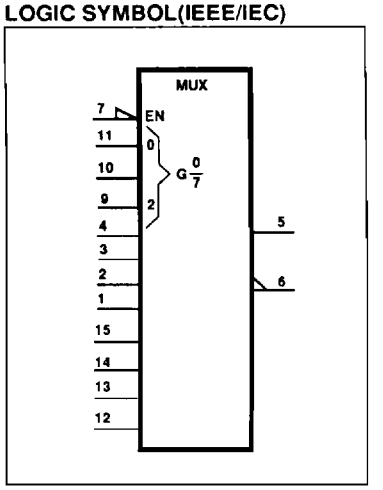


TOP VIEW

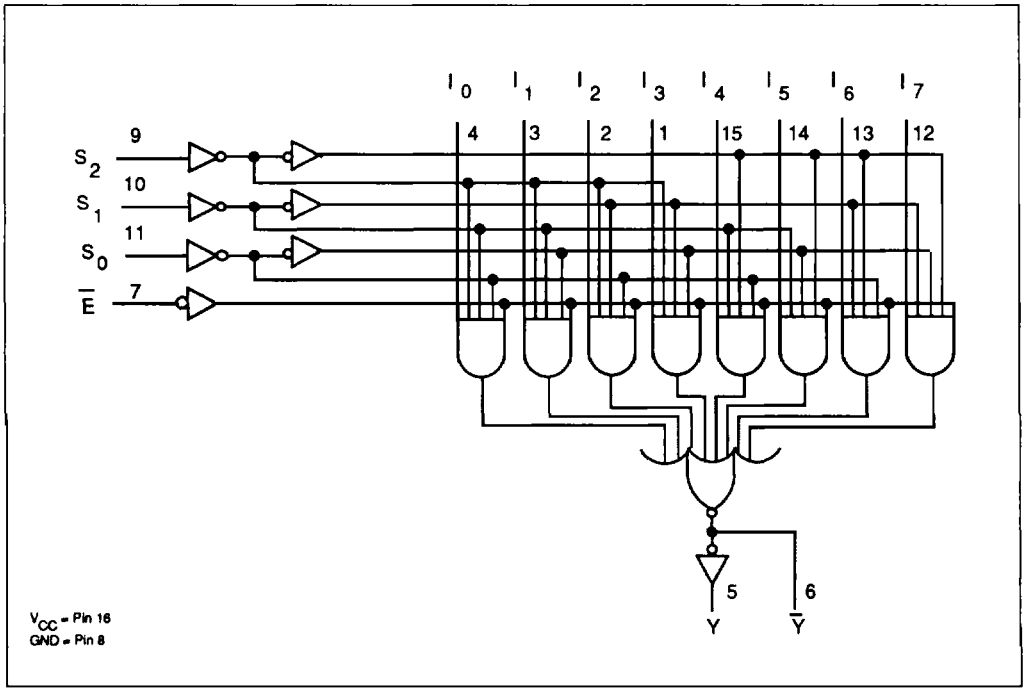
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{E}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F151	V_{CC} = MAX			13	18	mA
		I_{CCL}					15	20	mA
		I_{CCH}	74F151A	V_{CC} = MAX			18	25	mA
		I_{CCL}					17	25	mA

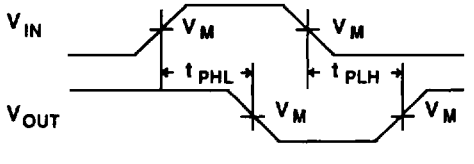
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

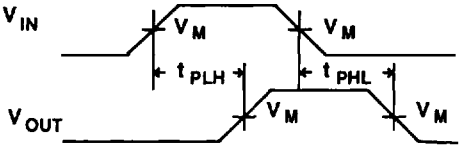
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F151	Waveform 1	3.0 3.0	4.5 4.5	6.5 6.5	2.5 3.0	9.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 2	2.0 1.0	4.0 2.5	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1,2	4.0 4.5	7.0 7.0	9.5 9.0	4.0 4.5	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1,2	4.0 2.0	6.5 4.5	9.0 7.0	3.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y		Waveform 1	6.0 4.0	8.0 5.5	10.0 7.0	5.5 4.0	11.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$		Waveform 1	3.5 4.0	5.0 5.5	6.5 7.5	3.5 4.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F151A	Waveform 1	2.5 2.5	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 2	2.0 1.0	4.0 2.0	7.0 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1,2	4.5 4.0	6.5 6.0	10.0 8.5	4.0 3.5	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1,2	3.5 2.5	5.5 4.5	8.5 7.0	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y		Waveform 1	4.0 3.0	6.5 5.0	9.0 7.0	3.5 3.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$		Waveform 1	2.5 2.0	4.5 3.5	6.5 5.5	2.5 1.5	7.0 6.0	ns

AC WAVEFORMS



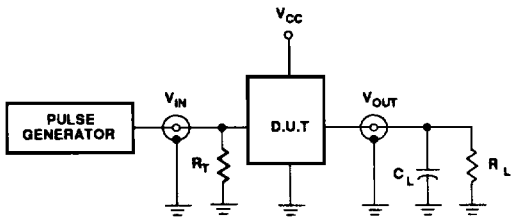
Waveform 1. For Inverting Outputs



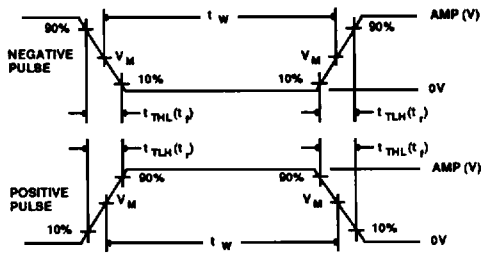
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.