Signetics

74F109
FLIP-FLOP

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops

Product Specification

FAST Products

DESCRIPTION

The 74F109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_0$) and Reset ($\overline{R}_0$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation.

The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together.

Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F109	125 MHz	12.3mA

ORDERING INFORMATION

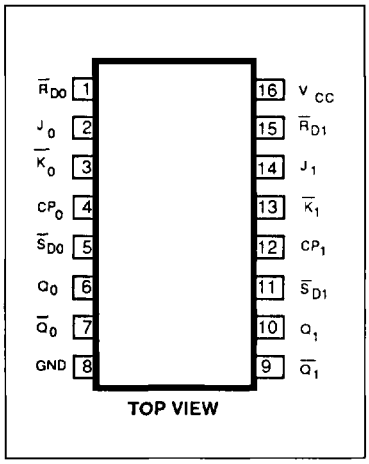
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F109N
16-Pin Plastic SO	N74F109D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
$\overline{K}_0$, $\overline{K}_1$	K inputs	1.0/1.0	20µA/0.6mA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/3.0	20µA/1.8mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/3.0	20µA/1.8mA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

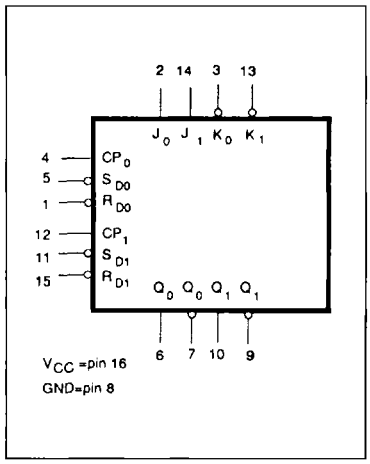
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

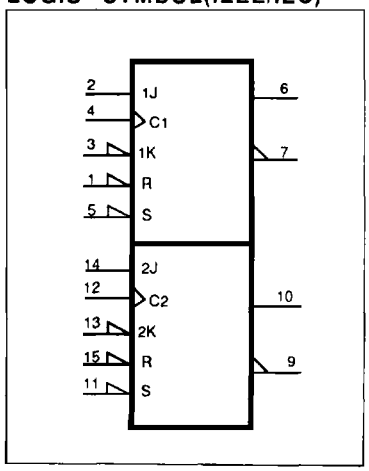


TOP VIEW

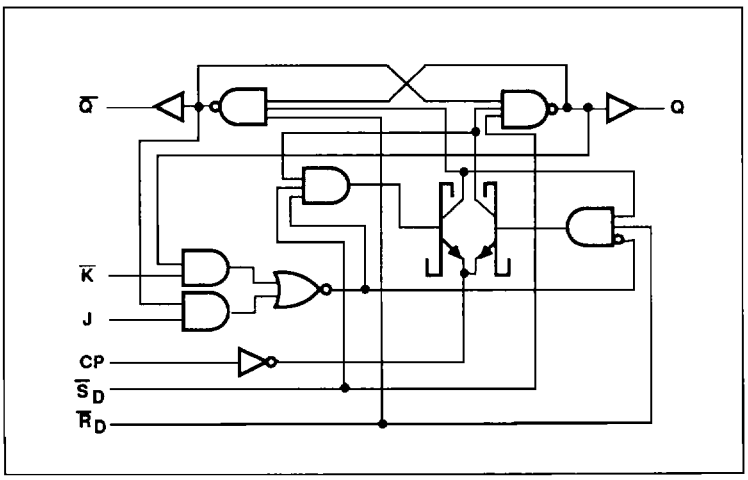
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H	H	Undetermined (Note)
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load "0" (Reset)
H	H	↑	h	h	H	L	Load "1" (Set)
H	H	↑	l	h	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
q=Lower case indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Note =Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$J, \overline{R}, CP_n$	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{S}_{Dn}, \overline{R}_{Dn}$					-1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			12.3	17	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

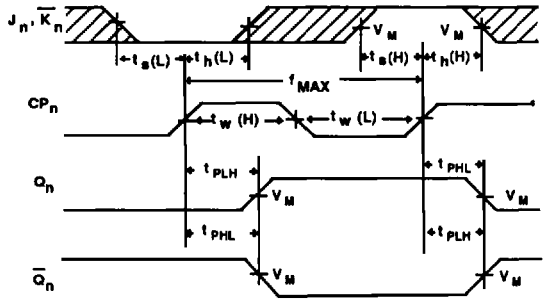
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	ns

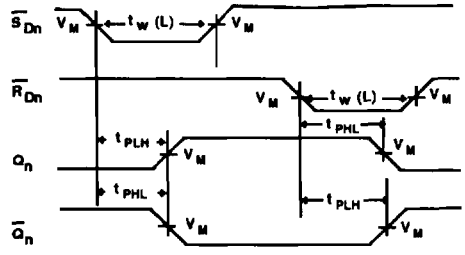
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, $\overline{K}_n$ to CP	Waveform 1	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, $\overline{K}_n$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_D$ or $\overline{R}_D$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time $\overline{S}_D$ or $\overline{R}_D$ to CP	Waveform 3	2.0			2.0		ns

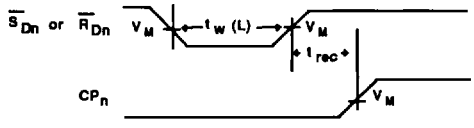
AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



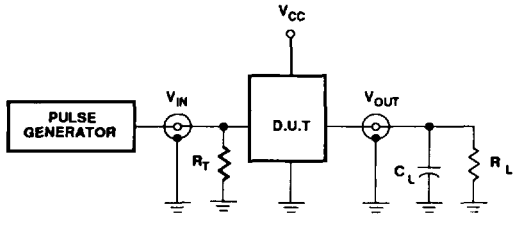
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



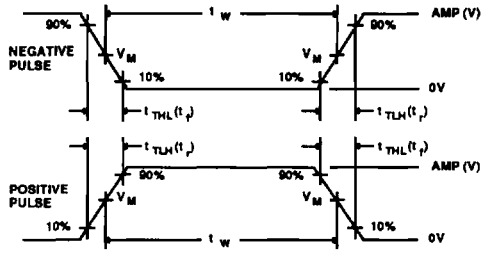
Waveform 3.
Propagation Delay for reset to output, reset pulse width, and recovery time for reset to clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.