DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT154
4-to-16 line decoder/demultiplexer

Product specification
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

4-to-16 line decoder/demultiplexer 74HC/HCT154

FEATURES

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs.
The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding “glitches” on the outputs, or it can be used for the expansion of the decoder.

The enable gate has two AND’ed inputs which must be LOW to enable the outputs.

The “154” can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay A_n, $\overline{E}_n$ to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	11	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	60	60	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	$\overline{Y}_0$ to $\overline{Y}_{15}$	outputs (active LOW)
18, 19	$\overline{E}_0$, $\overline{E}_1$	enable inputs (active LOW)
12	GND	ground (0 V)
23, 22, 21, 20	A_0 to A_3	address inputs
24	V_{CC}	positive supply voltage

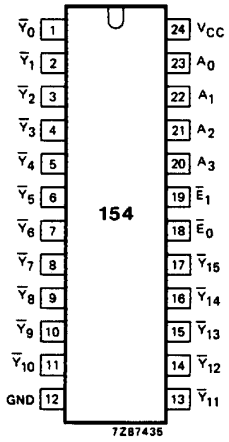


Fig.1 Pin configuration.

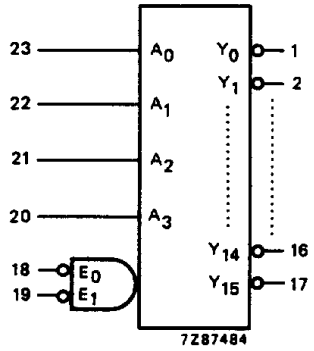
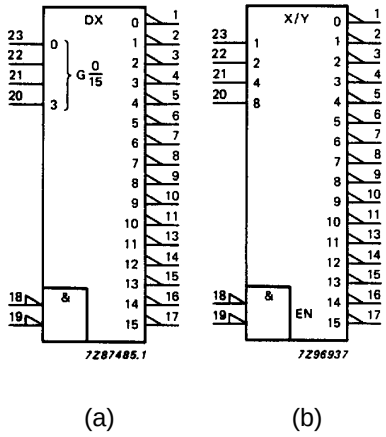


Fig.2 Logic symbol.



(a) (b)

Fig.3 IEC logic symbol.

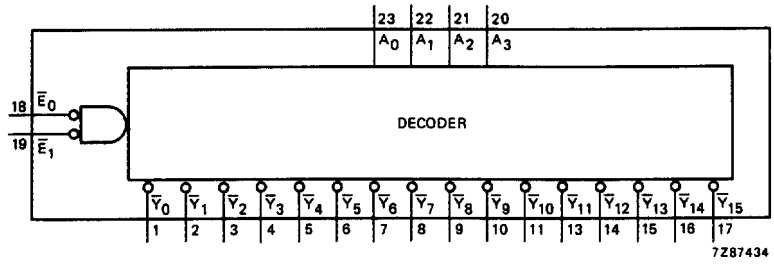


Fig.4 Functional diagram.

FUNCTION TABLE

		INPUTS				OUTPUTS														
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$	$\overline{Y}_{10}$	$\overline{Y}_{11}$	$\overline{Y}_{12}$	$\overline{Y}_{13}$	$\overline{Y}_{14}$	$\overline{Y}_{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
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L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
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L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

Note

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

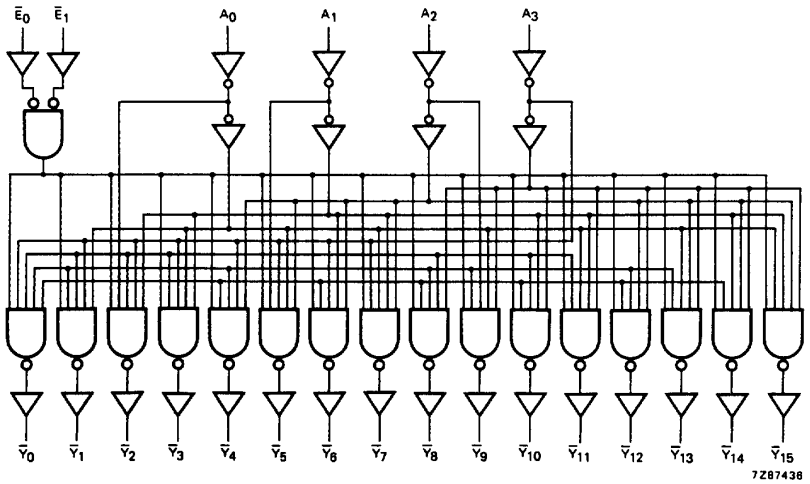


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

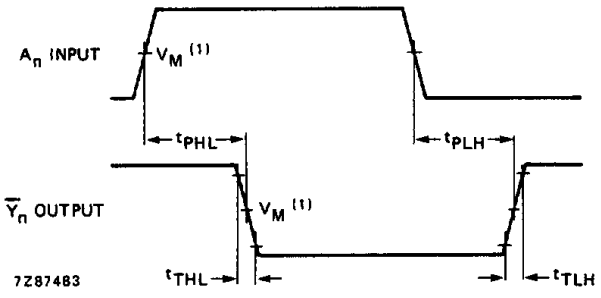
INPUT	UNIT LOAD COEFFICIENT
A_n	1.0
$\overline{E}_n$	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

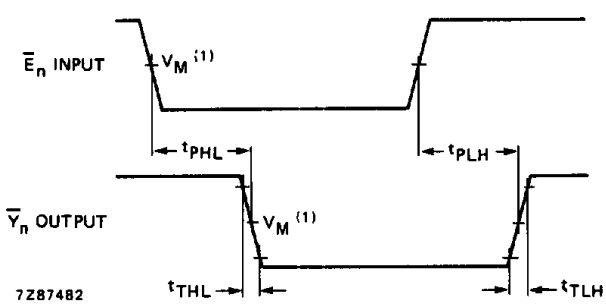
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay A_n to $\overline{Y}_n$		16	35		44		53	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$		15	32		40		48	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the address input (A_n) to output ($\overline{Y}_n$) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the enable input ($\overline{E}n$) to output ($\overline{Y}_n$) propagation delays and the output transition times.

APPLICATION INFORMATION

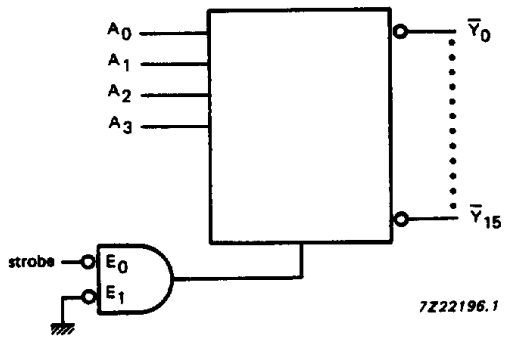


Fig.8 1-of-16 decoder; LOW level output is selected.

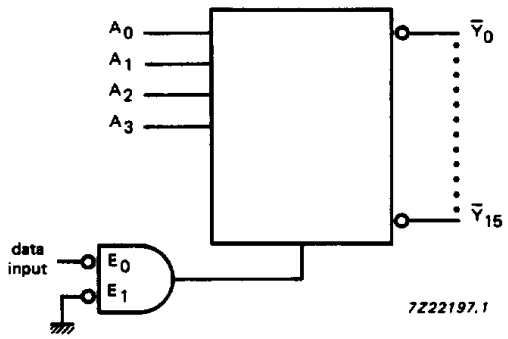


Fig.9 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

74HC/HCT154; 4-to-16 line decoder/demultiplexer

Information as of 2003-04-22

- Products
- MultiMarket Semiconductors
- Product Selector
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- Catalog by System
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General description

The 74HC/HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs.

The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding 'glitches' on the outputs, or it can be used for the expansion of the decoder.

The enable gate has two AND’ed inputs which must be LOW to enable the outputs.

The '154' can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

Features

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- I_{CC} category: MSI

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74HC/HCT154	4-to-16 line decoder/demultiplexer	9/1/1993	Product specification	7	57	Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

	Document	Description
1	HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications
2	HCT_PACKAGE_INFO	HC/T Package Info, The IC06 74HC/HCT/HCMOS Logic Package Information
3	HCT_PACKAGE_OUTLINES	HC/T Package Outlines, The IC06 74HC/HCT/HCMOS Logic Package Outlines

Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74HC154D	SOT137 (SO24)	4-to-16 Line Decoder/Demultiplexer	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC154DB	SOT340-1 (SSOP24)	4-to-16 Line Decoder/Demultiplexer	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC154N	SOT101-1 (DIP24)	4-to-16 Line Decoder/Demultiplexer	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC154PW	SOT355-1 (TSSOP24)	4-to-16 Line Decoder/Demultiplexer	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HCT154D	SOT137 (SO24)	4-to-16 Line Decoder/Demultiplexer; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT154DB	SOT340-1 (SSOP24)	4-to-16 Line Decoder/Demultiplexer; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT154N	SOT101-1 (DIP24)	4-to-16 Line Decoder/Demultiplexer; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT154PW	SOT355-1 (TSSOP24)	4-to-16 Line Decoder/Demultiplexer; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low

Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing Discretes packing info	Package	Device status	Buy online
74HC154D	74HC154D	9337 138 20652	Standard Marking * Bulk Pack, CECC	SOT137 (SO24)	Full production	order this -
	74HC154D-T	9337 138 20653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT137 (SO24)	Full production	order this -
74HC154DB	74HC154DB	9351 825 70112	Standard Marking * Bulk Pack	SOT340-1 (SSOP24)	Full production	order this -
	74HC154DB-T	9351 825 70118	Standard Marking * Reel Pack, SMD, 13"	SOT340-1 (SSOP24)	Full production	order this -

74HC154N	74HC154N	9336 710 20652	Standard Marking * Bulk Pack, CECC	SOT101-1 (DIP24)	Full production	order this -
74HC154PW	74HC154PW	9351 825 80112	Standard Marking * Bulk Pack	SOT355-1 (TSSOP24)	Full production	order this -
	74HC154PW-T	9351 825 80118	Standard Marking * Reel Pack, SMD, 13"	SOT355-1 (TSSOP24)	Full production	order this -
74HCT154D	74HCT154D	9337 138 30652	Standard Marking * Bulk Pack, CECC	SOT137 (SO24)	Full production	order this -
	74HCT154D-T	9337 138 30653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT137 (SO24)	Full production	order this -
74HCT154DB	74HCT154DB	9351 825 50112	Standard Marking * Bulk Pack	SOT340-1 (SSOP24)	Full production	order this -
	74HCT154DB-T	9351 825 50118	Standard Marking * Reel Pack, SMD, 13"	SOT340-1 (SSOP24)	Full production	order this -
74HCT154N	74HCT154N	9336 710 50652	Standard Marking * Bulk Pack, CECC	SOT101-1 (DIP24)	Full production	order this -
74HCT154PW	74HCT154PW	9351 825 60112	Standard Marking * Bulk Pack	SOT355-1 (TSSOP24)	Full production	order this -
	74HCT154PW-T	9351 825 60118	Standard Marking * Reel Pack, SMD, 13"	SOT355-1 (TSSOP24)	Full production	order this -

Products in the above table are all in production. Some variants are discontinued; click here for information on these variants.

Similar products

74HC/HCT154 links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

Support & tools

HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications(date 01-Mar-98)
HC/T User Guide(date 01-Nov-97)

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