

SN5423, SN5425, SN7423, SN7425 DUAL 4-INPUT NOR GATES WITH STROBE

SDLS082

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

description

These devices contain dual 4-input positive NOR gates with strobe. They perform the Boolean function:

$$Y = \overline{G(A + B + C + D)}$$

(with $1X$ and $1\bar{X}$ of '23 left open).

The SN5423 and the SN5425 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7423 and the SN7425 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open.
H = high level, L = low level, X = irrelevant

SN5423 . . . J OR W PACKAGE

SN7423 . . . N PACKAGE

(TOP VIEW)

1X	1	16	V _{CC}
1A	2	15	1X
1B	3	14	2D
1G	4	13	2C
1C	5	12	2G
1D	6	11	2B
1Y	7	10	2A
GND	8	9	2Y

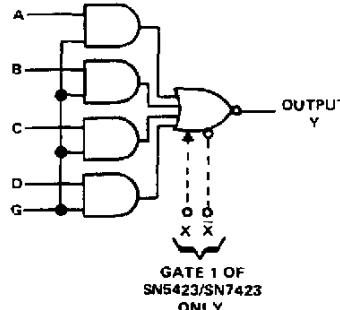
SN5425 . . . J OR W PACKAGE

SN7425 . . . N PACKAGE

(TOP VIEW)

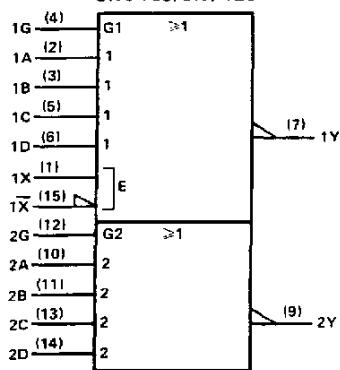
1A	1	14	V _{CC}
1B	2	13	2D
1G	3	12	2C
1C	4	11	2G
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y

logic diagram

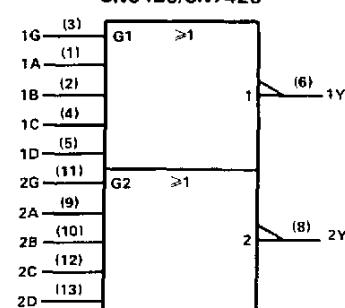


logic symbols[†]

SN5423/SN7423



SN5425/SN7425



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers are for J, N, or W packages.

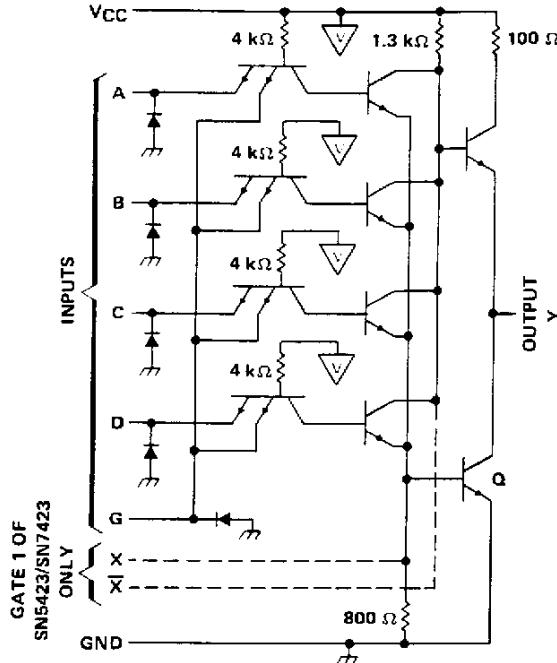
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SN5423, SN5425, SN7423, SNSN7425 DUAL 4-INPUT NOR GATES WITH STROBE

schematic (each gate)



NOTES: A. Component values shown are nominal.
 B. Both expander inputs are used simultaneously for expanding.
 C. If expander is not used leave X and X̄ open.
 D. A total of four expander gates can be connected to the expander inputs.

— VCC bus

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V _{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5423, SN5425 Circuits	— 55°C to 125°C
SN7423, SN7425 Circuits	0°C to 70°C
Storage temperature range	— 65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		'23, '25			UNIT
		MIN	NOM	MAX	
V _{CC} Supply voltage	54 Family	4.5	5	5.5	V
	74 Family	4.75	5	5.25	
V _{IH} High-level input voltage		2			V
V _{IL} Low-level input voltage			0.8		V
I _{OH} High-level output current			— 0.8		mA
I _{OL} Low-level output current	54 Family	16			mA
	74 Family	16			
T _A Operating free-air temperature range	54 Family	— 55	125		°C
	74 Family	0	70		

The '23 is designed for use with up to four '60 expanders.

SN5423, SN5425, SN7423, SN7425
DUAL 4-INPUT NOR GATES WITH STROBE

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT	
V_I		$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V	
V_{OH}		$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.8 \text{ mA}$	2.4	3.4		V	
V_{OL}		$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V	
I_I		$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA	
I_{IH}	data inputs	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40		
	strobe inputs				160	μA	
I_{IL}	data inputs	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6		
	strobe inputs				-6.4	mA	
$I_{OSS\$}$		$V_{CC} = \text{MAX}$	54 Family	-20	-55		
			74 Family	-18	-55	mA	
I_{CCH}		$V_{CC} = \text{MAX}$, All inputs at 0 V			8	mA	
I_{CCL}		$V_{CC} = \text{MAX}$, All inputs at 5 V			10	19	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and \bar{X} are open.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

electrical characteristics (SN5423 circuits) using expander inputs, $V_{CC} = 4.5 \text{ V}$, $T_A = -55^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_X	Expander current	$V_{X\bar{X}} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$			-3.5	mA
$V_{BE(Q)}$	Base-Emitter voltage of output transistor (Q)	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.41 \text{ mA}$, $R_{X\bar{X}} = 0$			1.1	V
V_{OH}	High-level output voltage	$I_{OH} = -0.4 \text{ mA}$, $I_X = 0.15 \text{ mA}$, $I_{\bar{X}} = -0.15 \text{ mA}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.3 \text{ mA}$, $R_{X\bar{X}} = 114 \Omega$	0.2	0.4		V

electrical characteristics (SN7423 circuits) using expander inputs, $V_{CC} = 4.75 \text{ V}$, $T_A = 0^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_X	Expander current	$V_{X\bar{X}} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$			-3.8	mA
$V_{BE(Q)}$	Base-Emitter voltage of output transistor (Q)	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.62 \text{ mA}$, $R_{X\bar{X}} = 0$			1	V
V_{OH}	High-level output voltage	$I_{OH} = -0.4 \text{ mA}$, $I_X = 0.27 \text{ mA}$, $I_{\bar{X}} = -0.27 \text{ mA}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 16 \text{ mA}$, $I_X + I_{\bar{X}} = 0.43 \text{ mA}$, $R_{X\bar{X}} = 130 \Omega$	0.2	0.4		V

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$, (see note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}		$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$	13	22		ns
t_{PHL}		$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$	8	15		ns

NOTE 3: Switching characteristics of the SN5423 and SN7424 are tested with the expander pins open.

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9763601QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/00403BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/00403BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN5423J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN5423J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN5425J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN5425J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN7423N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN7423N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN7425N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7425N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7425N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI
SN7425N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI
SN7425NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7425NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ5423J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5423J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5423W	OBsolete			16		TBD	Call TI	Call TI
SNJ5423W	OBsolete			16		TBD	Call TI	Call TI
SNJ5425J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5425J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ5425W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ5425W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

temperature.

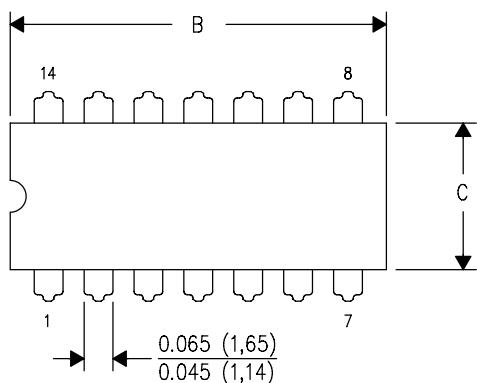
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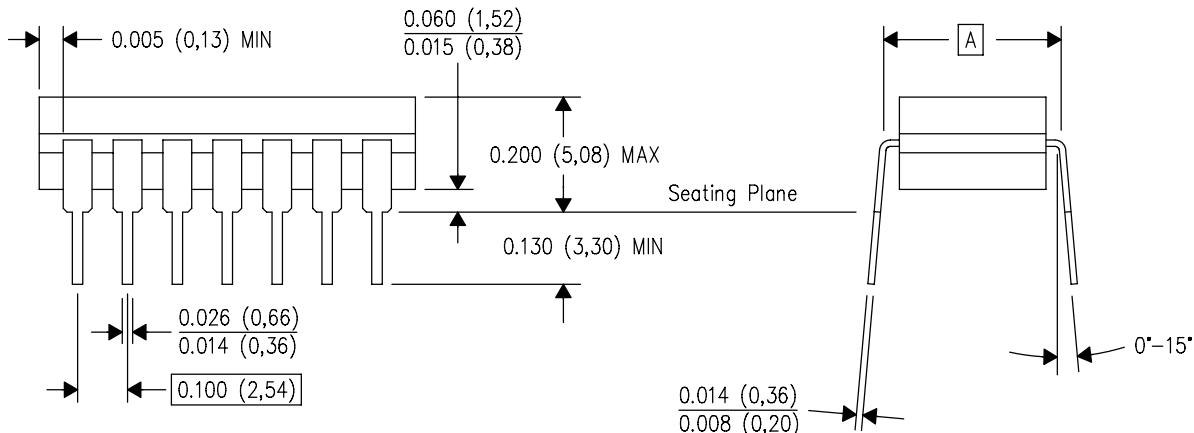
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

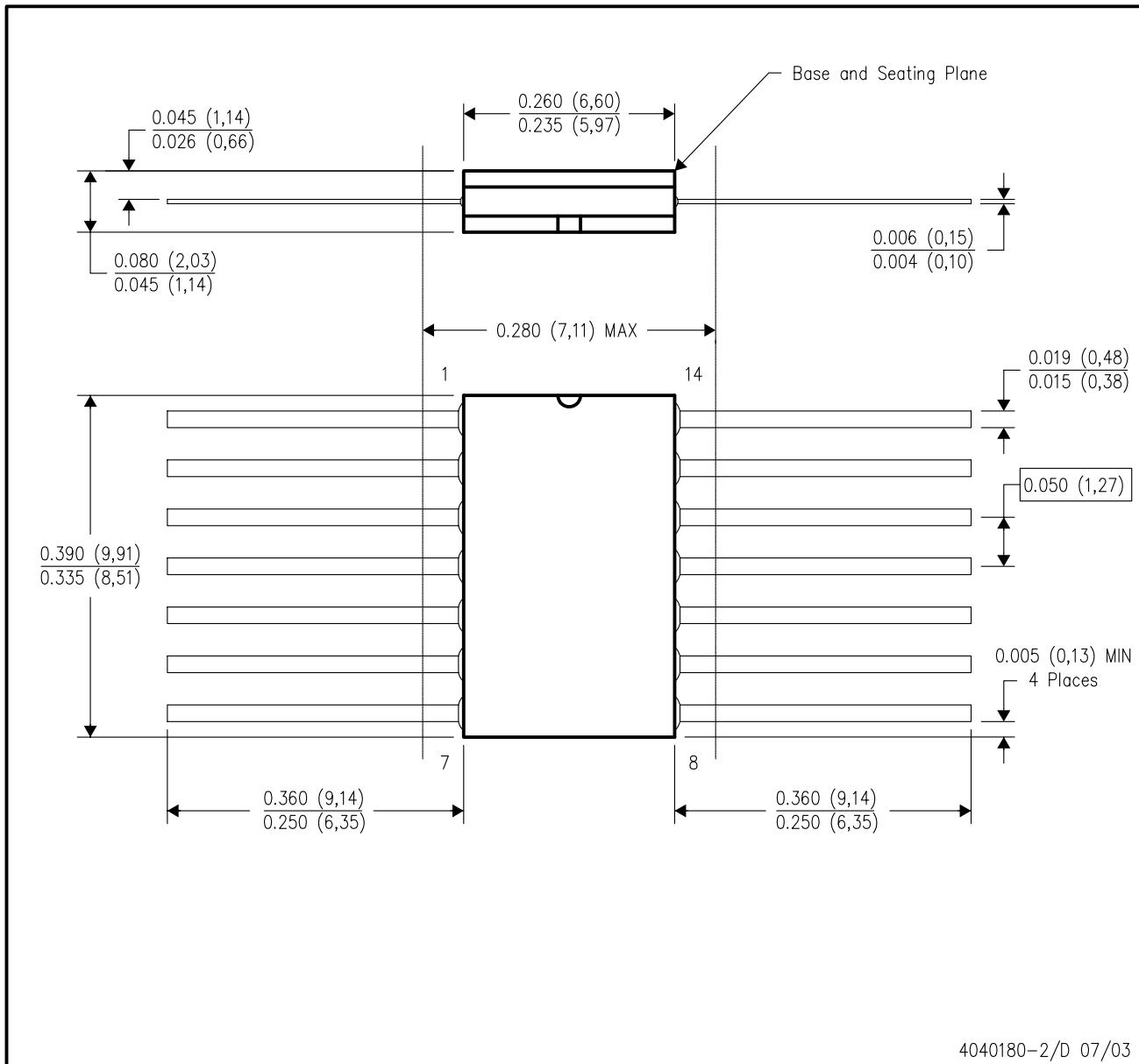


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



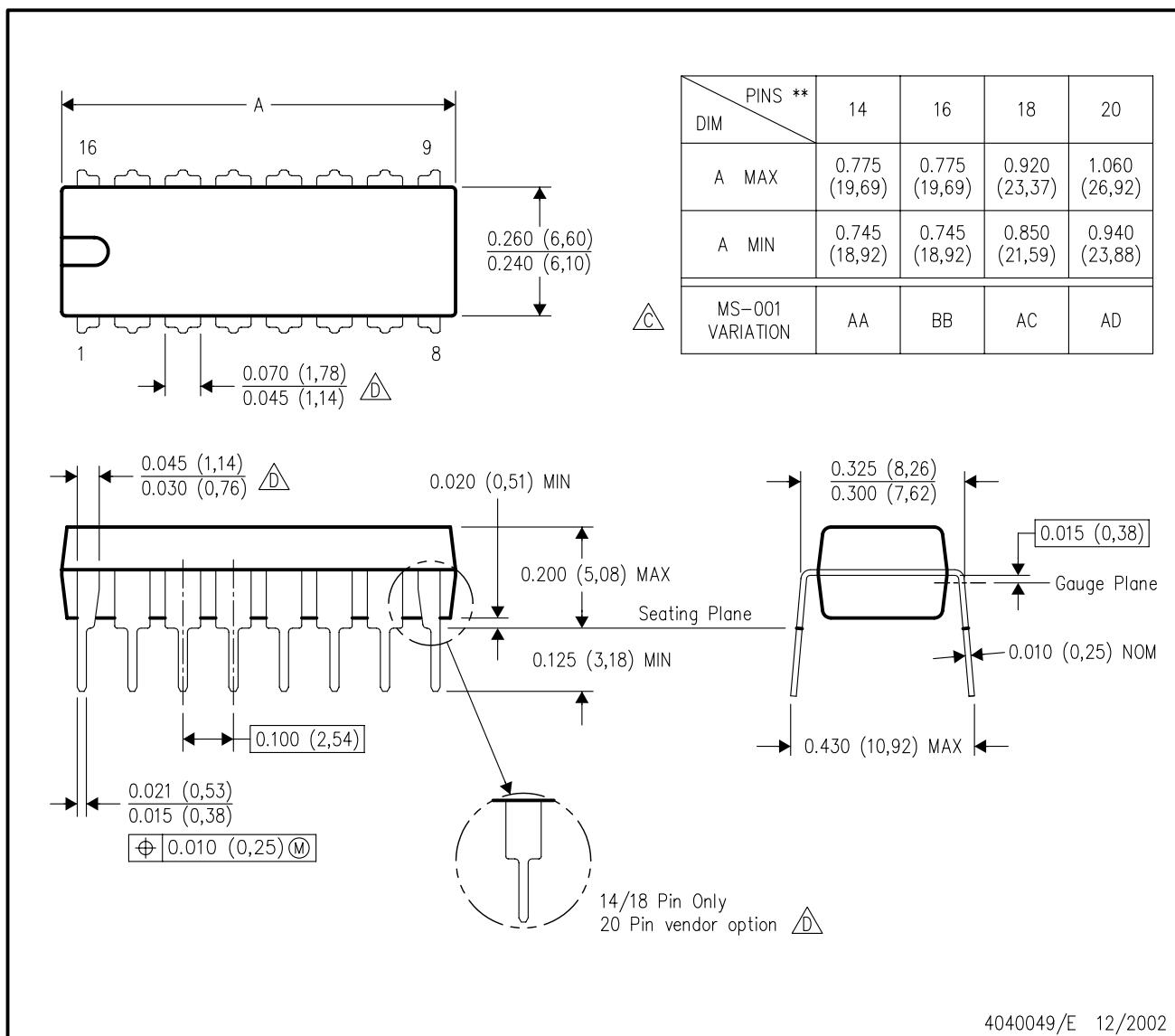
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9763601QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9763601QE A SNJ5423J	Samples
JM38510/00403BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00403BCA	Samples
JM38510/00403BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00403BCA	Samples
M38510/00403BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00403BCA	Samples
M38510/00403BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00403BCA	Samples
SN5425J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5425J	Samples
SN5425J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5425J	Samples
SN7423N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN7423N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN7425N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7425N	Samples
SN7425N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7425N	Samples
SN7425N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7425N3	OBsolete	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7425NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7425N	Samples
SN7425NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7425N	Samples
SNJ5423J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9763601QE A SNJ5423J	Samples
SNJ5423J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9763601QE A SNJ5423J	Samples
SNJ5423W	OBsolete			16		TBD	Call TI	Call TI	-55 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
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SNJ5425J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5425J	Samples
SNJ5425J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5425J	Samples
SNJ5425W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5425W	Samples
SNJ5425W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5425W	Samples

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN5423, SN5425, SN7423, SN7425 :

- Catalog: [SN7423, SN7425](#)
- Military: [SN5423, SN5425](#)

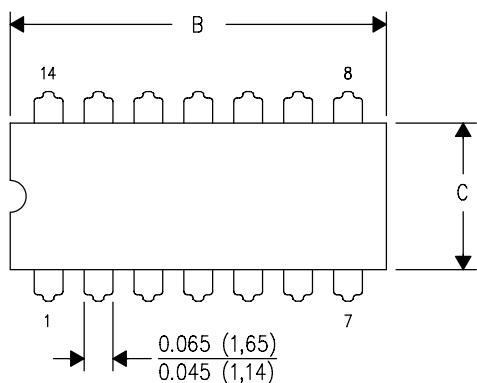
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

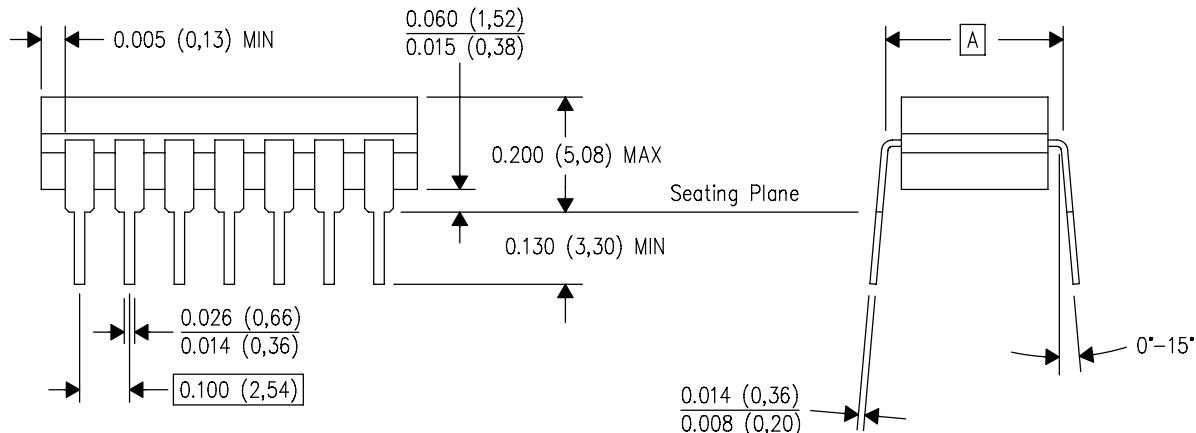
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

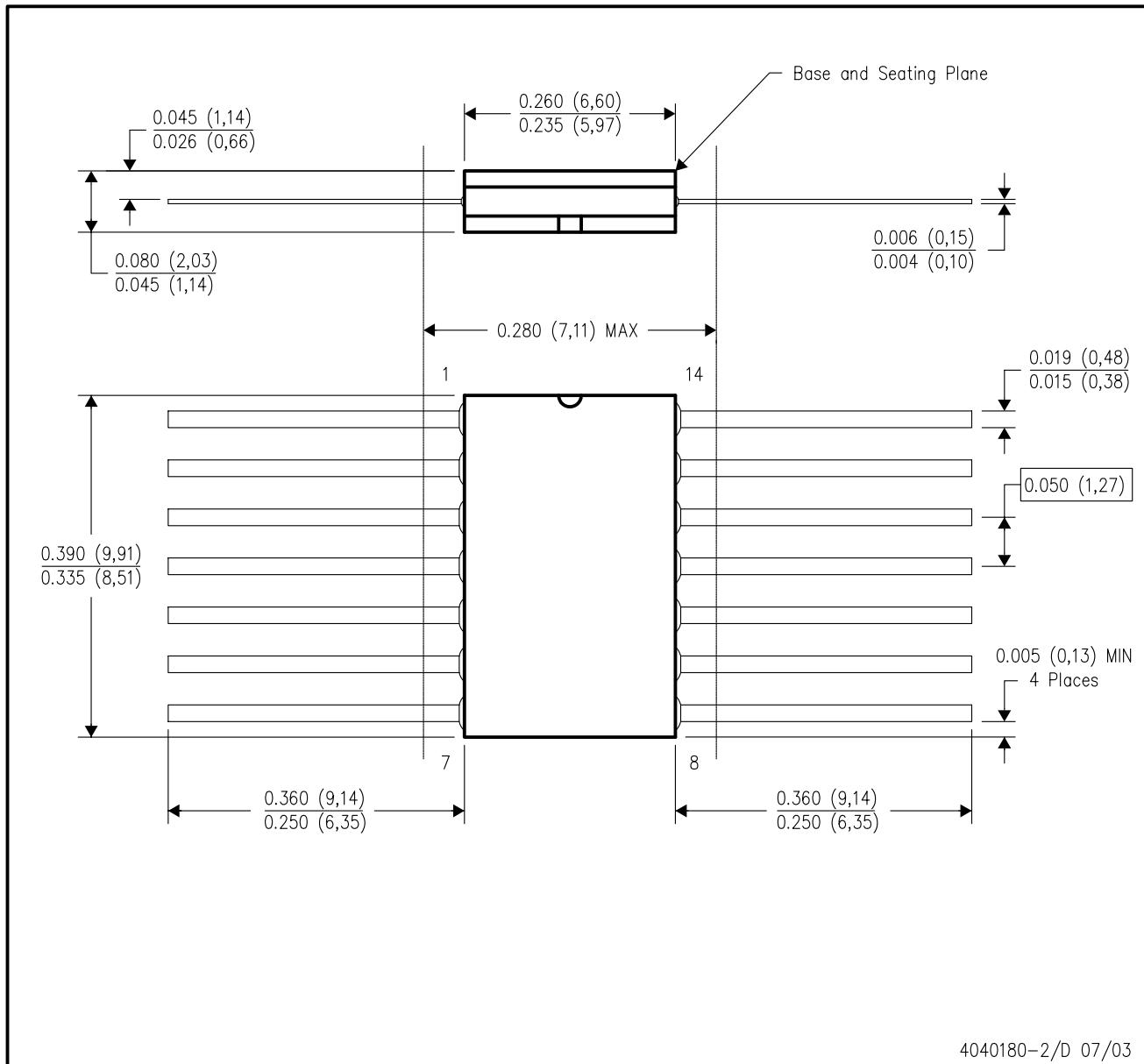


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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



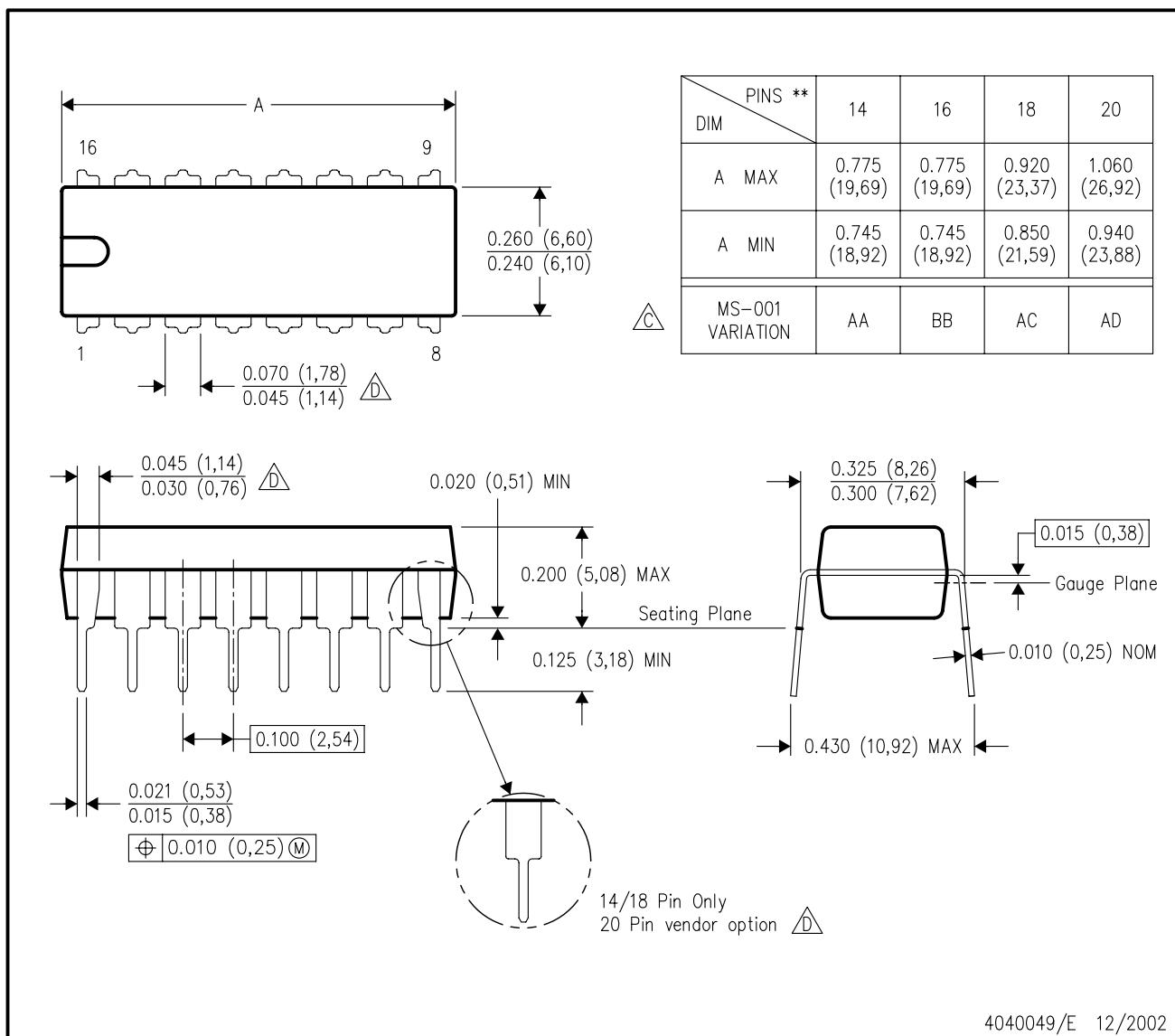
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- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



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