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Jameco Part Number 49832TI

SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

DECEMBER 1972—REVISED MARCH 1988

SN54180 . . . J OR W PACKAGE
SN74180 . . . N PACKAGE

(TOP VIEW)

FUNCTION TABLE

INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of -55°C to 125°C ; and the SN74180 is characterized for operation from 0°C to 70°C .

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54180			SN74180			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

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SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54180			SN74180			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH} High-level input voltage			2		2		2	V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μ A	2.4	3.3		2.4	3.3		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	Any data input			40			40	
	Even or odd input	V _{CC} = MAX, V _I = 2.4 V		80			80	μ A
I _{IL} Low-level input current	Any data input			-1.6			-1.6	
	Even or odd input	V _{CC} = MAX, V _I = 0.4 V		-3.2			-3.2	mA
I _{OS} Short-circuit output current [§]	V _{CC} = MAX		-20	-55	-18	-55	-55	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2	34	49		34	49	56	mA

NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time.

2

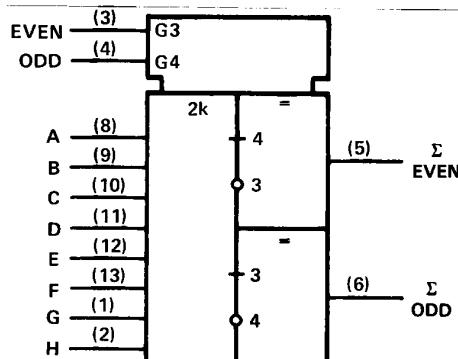
TTL Devices

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}		Σ Even		40	60		
t _{PHL}	Data		C _L = 15 pF, R _L = 400 Ω , Odd input grounded, See Note 3	45	68		ns
t _{PLH}		Σ Odd		32	48		
t _{PHL}	Data			25	38		
t _{PLH}		Σ Even		32	48		
t _{PHL}	Data		C _L = 15 pF, R _L = 400 Ω , Even input grounded, See Note 3	25	38		
t _{PLH}		Σ Odd		40	60		
t _{PHL}				45	68		
t _{PLH}	Even or Odd	Σ Even or Σ Odd	C _L = 15 pF, R _L = 400 Ω , See Note 3	13	20		
t _{PHL}				7	10		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

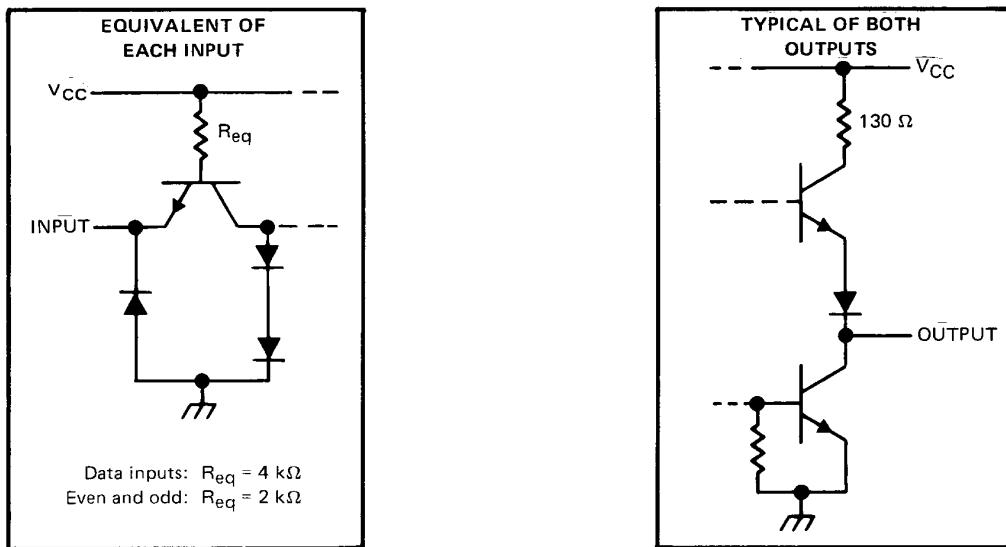
logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54180, SN74180
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

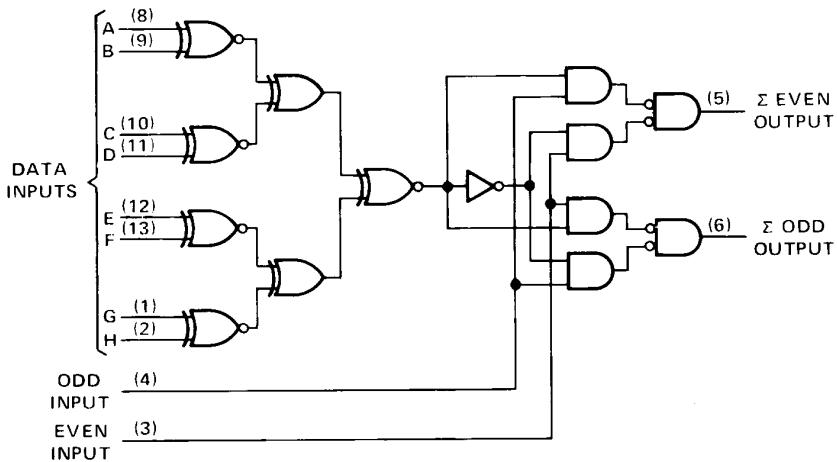
schematics of inputs and outputs



2

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logic diagram (positive logic)



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