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Jameco Part Number 45831FSC

## MM74HC373

### 3-STATE Octal D-Type Latch

#### General Description

The MM74HC373 high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what

signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

#### Features

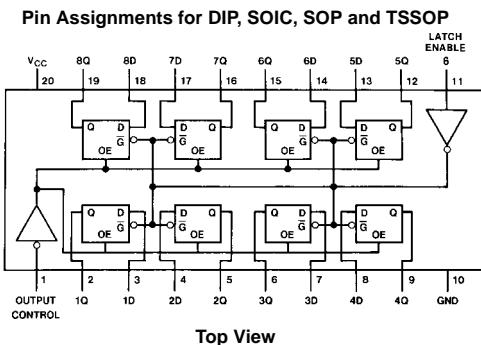
- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1  $\mu$ A maximum
- Low quiescent current: 80  $\mu$ A maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

#### Ordering Code:

Order Number	Package Number	Package Description
MM74HC373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



#### Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

H = HIGH Level

L = LOW Level

$Q_0$  = Level of output before steady-state input conditions were established.

Z = High Impedance

**Absolute Maximum Ratings**<sup>(Note 1)</sup>

(Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC}$ +1.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC}$ +0.5V
Clamp Diode Current ( $I_{IK}$ , $I_{OK}$ )	±20 mA
DC Output Current, per pin ( $I_{OUT}$ )	±35 mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±70 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	600 mW
(Note 3)	500 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	260°C
(Soldering 10 seconds)	

**Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}$ , $V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	-40	+85	°C
Input Rise or Fall Times ( $t_r$ , $t_f$ )			
$V_{CC} = 2.0V$	1000	ns	
$V_{CC} = 4.5V$	500	ns	
$V_{CC} = 6.0V$	400	ns	

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0 \text{ mA}$ $ I_{OUT}  \leq 7.8 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0 \text{ mA}$ $ I_{OUT}  \leq 7.8 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	µA
$I_{OZ}$	Maximum 3-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or $V_{IL}$ , $OC = V_{IH}$ $V_{OUT} = V_{CC}$ or GND	6.0V		±0.5	±5	±10	µA
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	µA

**Note 4:** For a power supply of  $5V \pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $t_r = t_f = 6$  ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Data to Q	$C_L = 45$ pF	18	25	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, LE to Q	$C_L = 45$ pF	21	30	ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time	$R_L = 1$ k $\Omega$ $C_L = 45$ pF	20	28	ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time	$R_L = 1$ k $\Omega$ $C_L = 5$ pF	18	25	ns
$t_S$	Minimum Set Up Time			5	ns
$t_H$	Minimum Hold Time			10	ns
$t_W$	Minimum Pulse Width		9	16	ns

## AC Electrical Characteristics

$V_{CC} = 2.0\text{--}6.0V$ ,  $C_L = 50$  pF,  $t_r = t_f = 6$  ns (unless otherwise specified)

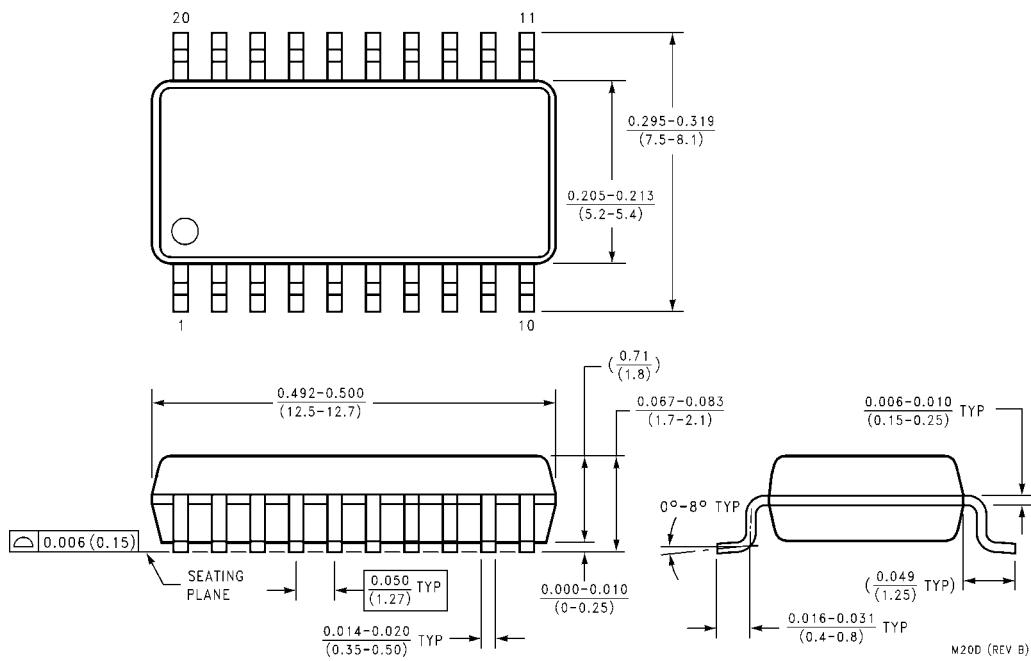
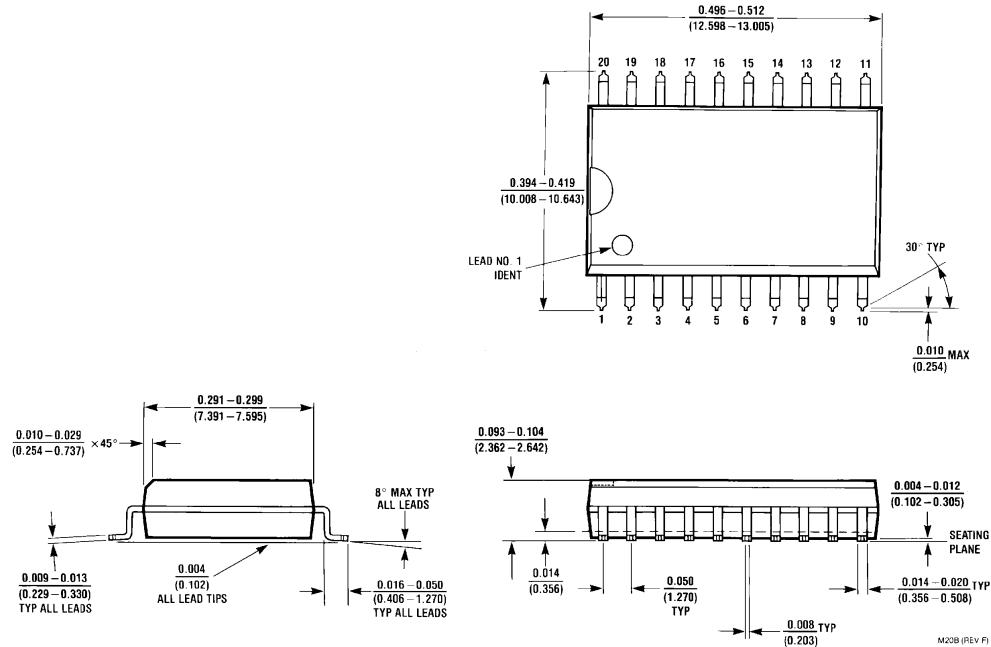
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Guaranteed Limits	Units
				Typ	$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$		
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Data to Q	$C_L = 50$ pF	2.0V	50	150	188	225	ns
		$C_L = 150$ pF	2.0V	80	200	250	300	ns
		$C_L = 50$ pF	4.5V	22	30	37	45	ns
		$C_L = 150$ pF	4.5V	30	40	50	60	ns
		$C_L = 50$ pF	6.0V	19	26	31	39	ns
		$C_L = 150$ pF	6.0V	26	35	44	53	ns
		$C_L = 50$ pF	2.0V	63	175	220	263	ns
		$C_L = 150$ pF	2.0V	110	225	280	338	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, LE to Q	$C_L = 50$ pF	4.5V	25	35	44	52	ns
		$C_L = 150$ pF	4.5V	35	45	56	68	ns
		$C_L = 50$ pF	6.0V	21	30	37	45	ns
		$C_L = 150$ pF	6.0V	28	39	49	59	ns
		$R_L = 1$ k $\Omega$						
		$C_L = 50$ pF	2.0V	50	150	188	225	ns
		$C_L = 150$ pF	2.0V	80	200	250	300	ns
		$C_L = 50$ pF	4.5V	21	30	37	45	ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time	$C_L = 150$ pF	4.5V	30	40	50	60	ns
		$C_L = 50$ pF	6.0V	19	26	31	39	ns
		$C_L = 150$ pF	6.0V	26	35	44	53	ns
		$R_L = 1$ k $\Omega$						
		$C_L = 50$ pF	2.0V	50	150	188	225	ns
		$C_L = 150$ pF	2.0V	80	200	250	300	ns
		$C_L = 50$ pF	4.5V	21	30	37	45	ns
		$C_L = 150$ pF	4.5V	30	40	50	60	ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time	$C_L = 50$ pF	6.0V	19	26	31	39	ns
		$C_L = 150$ pF	6.0V	19	26	31	39	ns
		$R_L = 1$ k $\Omega$						
		$C_L = 50$ pF	2.0V	50	150	188	225	ns
		$C_L = 150$ pF	2.0V	21	30	37	45	ns
		$C_L = 50$ pF	4.5V	19	26	31	39	ns
		$C_L = 150$ pF	4.5V	19	26	31	39	ns
		$C_L = 50$ pF	6.0V	19	26	31	39	ns
$t_S$	Minimum Set Up Time		2.0V		50	60	75	ns
			4.5V		9	13	15	ns
			6.0V		9	11	13	ns
			2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
			2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
$t_H$	Minimum Hold Time		6.0V	9	14	18	20	ns
			2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
			2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
			2.0V	25	60	75	90	ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time	$C_L = 50$ pF	4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per latch) $OC = V_{CC}$ $OC = GND$		30 50				pF pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

## AC Electrical Characteristics (Continued)

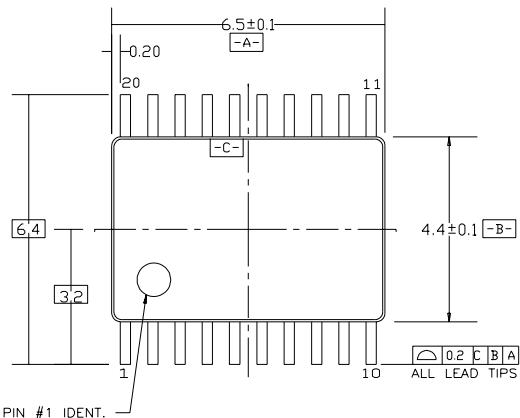
Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	Units
				Typ	Guaranteed Limits			
C <sub>OUT</sub>	Maximum Output Capacitance			15	20	20	20	pF

**Note 5:** C<sub>PD</sub> determines the no load dynamic power consumption, P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f + I<sub>CC</sub> V<sub>CC</sub>, and the no load dynamic current consumption, I<sub>S</sub> = C<sub>PD</sub> V<sub>CC</sub> f + I<sub>CC</sub>.

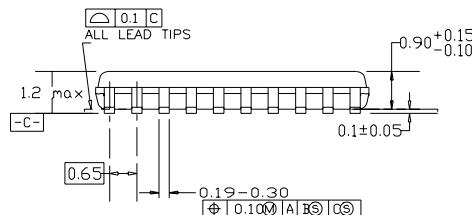
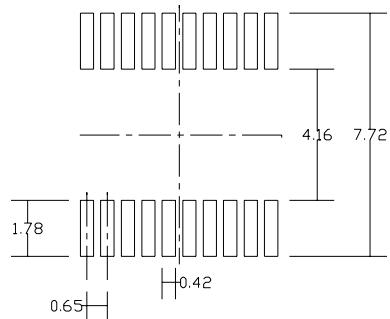
**Physical Dimensions** inches (millimeters) unless otherwise noted



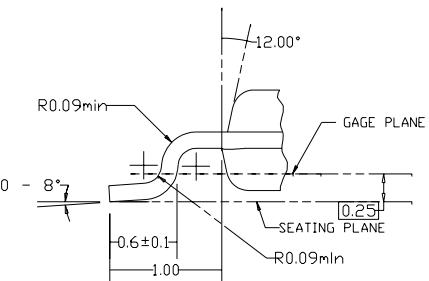
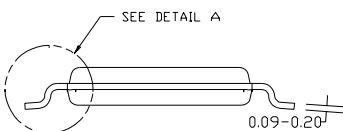
## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



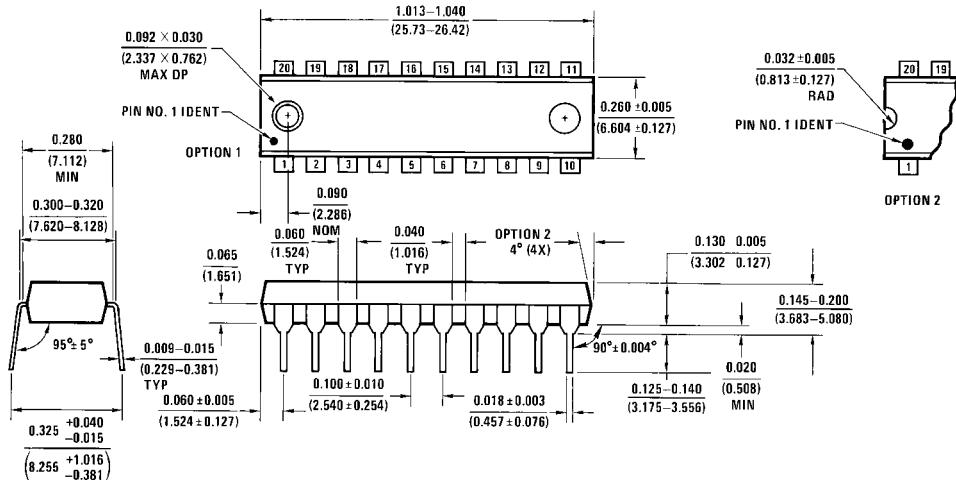
DETAIL A

## NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC,  
REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH,  
AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A

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