**Philips Semiconductors-Signetics**

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# FAST 74F257, 74F257A
# Data Selectors/Multiplexers

**74F257 Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)**
**74F257A Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F257 | 4.3ns | 12mA |
| 74F257A | 4.3ns | 12mA |

## FEATURE

- **Multifunction capability**
- **Non-inverting data path**
- **3-state outputs**
- **See 'F258A for inverting version**

## DESCRIPTION

The 74F257/74F257A has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Select (S) input. The $I_{0n}$ inputs are selected when the common Select input is Low and the $I_{1n}$ inputs are selected when the common Select input is High. Data appears at the outputs in true non-inverted form from the selected inputs. The 'F257/'F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the common Select input. Outputs are forced to a high impedance "off" state when the Output Enable ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum ratings if the outputs were tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices were tied together. The 74F257A is the faster version of 74F257.

## ORDERING INFORMATION

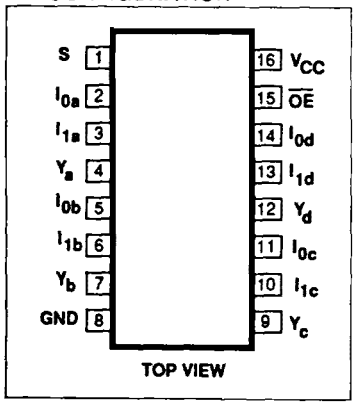
| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V±10%; $T_A$ = 0°C to +70°C |
|---|---|
| 16-Pin Plastic DIP | N74F257N, N74F257AN |
| 16-Pin Plastic SO | N74F257D, N74F257AD |

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

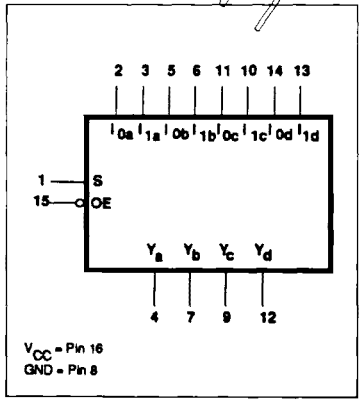
| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| $I_{0n}$, $I_{1n}$ | Data inputs | 1.0/1.0 | 20µA/0.6mA |
| S | Common Select input | 1.0/1.0 | 20µA/0.6mA |
| $\overline{OE}$ | Output Enable input (active Low) | 1.0/1.0 | 20µA/0.6mA |
| $\overline{Y}_a$ - $\overline{Y}_d$ | Data outputs | 150/33 | 3.0mA/20mA |

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

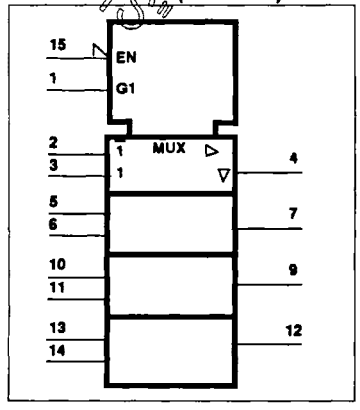
## PIN CONFIGURATION



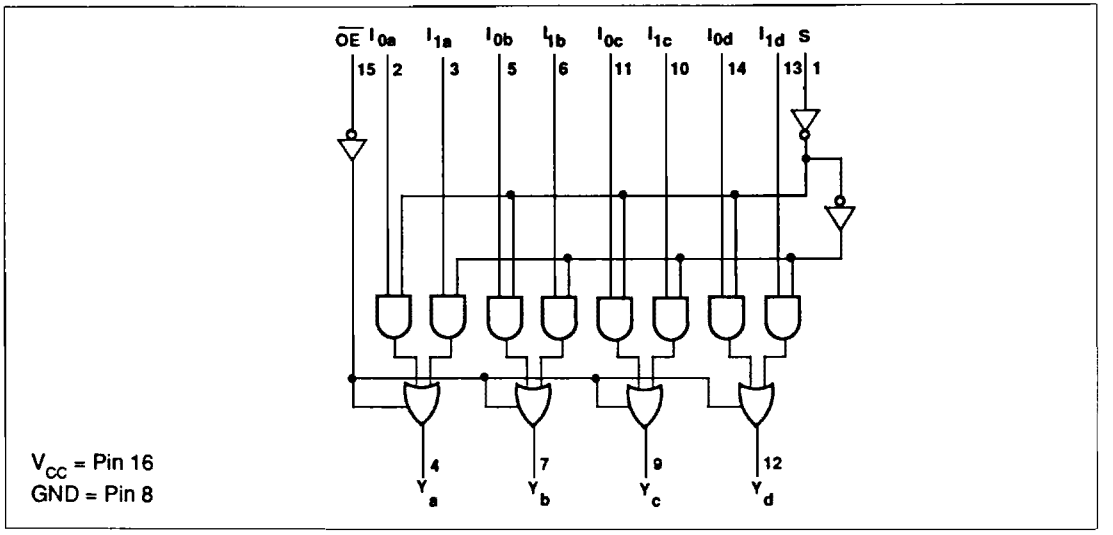

## LOGIC SYMBOL




## LOGIC SYMBOL(IEEE/IEC)



## LOGIC DIAGRAM

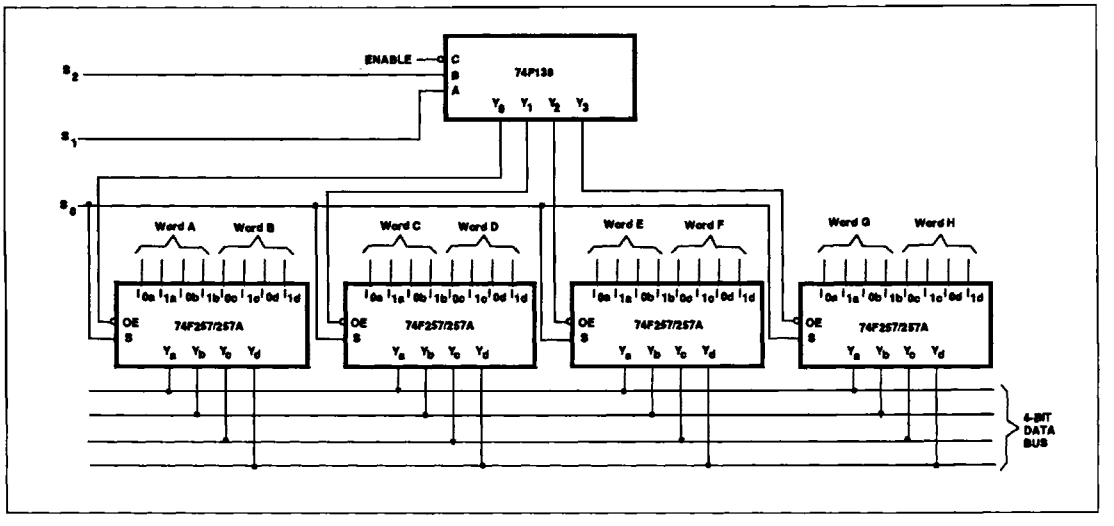



## FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | S | $I_0$ | $I_1$ | $\overline{Y}$ |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

## APPLICATION




## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | -0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | -0.5 to +7.0 | V |
| $I_{IN}$ | Input current | -30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in High output state | -0.5 to +$V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in Low output state | 48 | mA |
| $T_A$ | Operating free-air temperature range | 0 to +70 | °C |
| $T_{STG}$ | Storage temperature | -65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | -18 | mA |
| $I_{OH}$ | High-level output current | | | -3 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $T_A$ | Operating free-air temperature range | 0 | | 70 | °C |

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS[1] | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OH}$ = MAX | ±10%$V_{CC}$ | 2.4 | | | V |
| | | | ±5%$V_{CC}$ | 2.7 | 3.3 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OL}$ = MAX | ±10%$V_{CC}$ | | 0.35 | 0.50 | V |
| | | | ±5%$V_{CC}$ | | 0.35 | 0.50 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | -0.73 | -1.2 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ =MAX, $V_I$ = 7.0V | | | | 100 | µA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.5V | | | | -0.6 | mA |
| $I_{OZH}$ | Off state output current, High-level voltage applied | $V_{CC}$ = MAX, $V_O$ = 2.7V | | | | 50 | µA |
| $I_{OZL}$ | Off state output current, Low-level voltage applied | $V_{CC}$ = MAX, $V_O$ = 0.5V | | | | -50 | µA |
| $I_{OS}$ | Short circuit output current[3] | $V_{CC}$ = MAX | | -60 | | -150 | mA |
| $I_{CC}$ | Supply current[4] (total) | 'F257 | $I_{CCH}$ | $V_{CC}$ = MAX | | 9.0 | 16.0 | mA |
| | | | $I_{CCL}$ | | | 14.5 | 22.0 | mA |
| | | | $I_{CCZ}$ | | | 15.0 | 23.0 | mA |
| | | 'F257A | $I_{CCH}$ | $V_{CC}$ = MAX | | 9.0 | 15.0 | mA |
| | | | $I_{CCL}$ | | | 14.5 | 22.0 | mA |
| | | | $I_{CCZ}$ | | | 15.0 | 23.0 | mA |

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed lasty.
4. Measure $I_{CC}$ with all outputs open and inputs grounded.

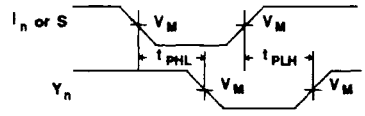
## AC ELECTRICAL CHARACTERISTICS for 'F257

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C, $V_{CC}$ = 5V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$I_n$ to $Y_n$ | Waveform 1 | 3.0<br>2.0 | 4.5<br>3.5 | 6.0<br>5.5 | 3.0<br>2.0 | 7.0<br>6.5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>S to $Y_n$ | Waveform 1 | 4.5<br>3.5 | 8.0<br>6.0 | 13.0<br>8.5 | 4.5<br>3.5 | 15.0<br>9.5 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable time<br>to High or Low level | Waveform 2<br>Waveform 3 | 3.0<br>3.0 | 6.0<br>6.0 | 7.5<br>7.5 | 3.0<br>3.0 | 8.5<br>8.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable time<br>from High or Low level | Waveform 2<br>Waveform 3 | 2.0<br>2.0 | 4.0<br>3.5 | 6.0<br>6.0 | 2.0<br>2.0 | 7.0<br>7.0 | ns |

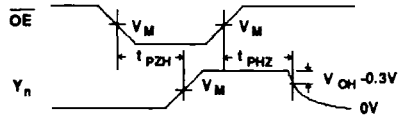
## AC ELECTRICAL CHARACTERISTICS for 'F257A

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C, $V_{CC}$ = 5V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$I_n$ to $Y_n$ | Waveform 1 | 3.0<br>2.0 | 4.5<br>3.5 | 6.0<br>5.0 | 3.0<br>2.0 | 7.0<br>6.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>S to $Y_n$ | Waveform 1 | 5.5<br>4.0 | 7.5<br>5.5 | 9.5<br>7.0 | 5.0<br>4.0 | 10.5<br>8.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable time<br>to High or Low level | Waveform 2<br>Waveform 3 | 4.5<br>4.5 | 6.5<br>6.0 | 7.5<br>7.5 | 4.5<br>4.5 | 8.5<br>8.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable time<br>from High or Low level | Waveform 2<br>Waveform 3 | 2.0<br>2.0 | 4.0<br>3.5 | 5.5<br>5.5 | 2.0<br>2.0 | 6.0<br>6.0 | ns |

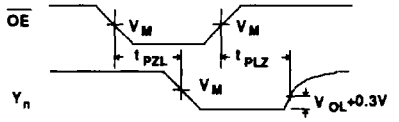
## AC WAVEFORMS




Waveform 1. Propagation Delay, Data and Select to Output



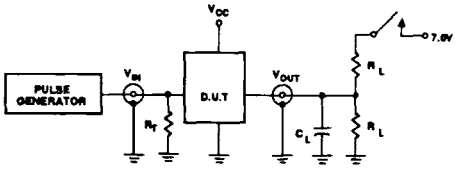

Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level




Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M$ = 1.5V.

## TEST CIRCUIT AND WAVEFORMS




Test Circuit For 3-State Outputs

### SWITCH POSITION

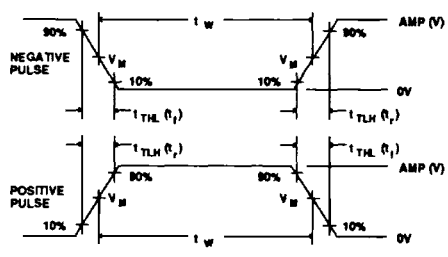
| TEST | SWITCH |
|---|---|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open |

DEFINITIONS

$R_L$ = Load resistor; see AC CHARACTERISTICS for value.

$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.




$V_M$ = 1.5V

Input Pulse Definition

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | $t_W$ | $t_{TLH}$ | $t_{THL}$ |
| 74F | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |