SILICON STACKED GATE CMOS

262,144 WORD x 16 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

Description

The TC574096D is a 262,144 word x 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory. The TC574096D has a JEDEC standard pin configuration. This product is available in a 40-pin standard cerdip package.

The TC574096D is fabricated using CMOS technology. Advanced circuit techniques result in both high speed and low power features with a maximum operating current of 70mA/10MHz and access times of 100ns/120ns/150ns.

Programming is achieved by using a high speed programming mode.

Features

- Peripheral circuit : CMOS
  Memory cell : NMOS
- Access time

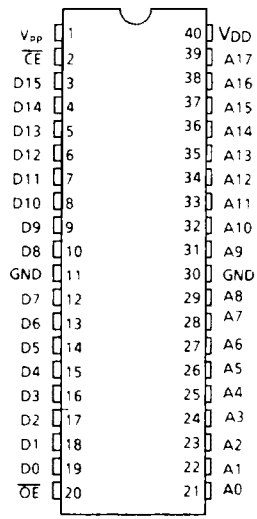
	-10	-120	-150
V_{DD}	5V±5%	5V±10%	
t_{ACC}	100ns	120ns	150ns

- Low power dissipation
  - Active : 70mA/10MHz
  - Standby : 100μA
- Single 5V power supply
- Fully static operation
- High speed programming mode : t_{PW} = 50μs
- Inputs and outputs TTL compatible
- JEDEC standard 40-pin DIP cerdip package :
  - WDIP40-G-600B

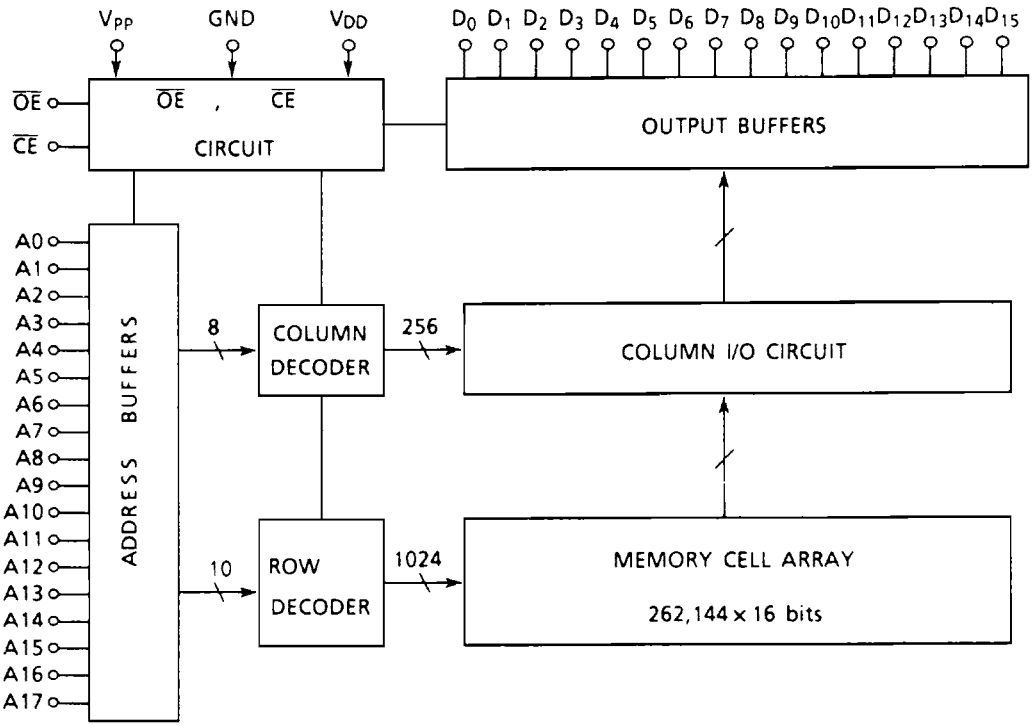
Pin Names

A0 ~ A17	Address Inputs
D0 ~ D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply Voltage (+5V)
V_{PP}	Program Supply Voltage
GND	Ground

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D0 ~ D15	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*				Standby
Program	L	H	12.50V	6.25V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	
V_{IN}	Input Voltage	-0.6 ~ 7.0	
V_{IN}(A9)	Input Voltage (A9)	-0.6 ~ 13.5	
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{DD} + 0.5	
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STRG}	Storage Temperature	-65 ~ 125	°C
T_{OPR}	Operating Temperature	0 ~ 70	

Read Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	TC574096D-10			TC574096D-120/150			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	4.75	5.00	5.25	4.50	5.00	5.50	
V_{PP}	Program Supply Voltage	0	–	V_{DD} + 0.6	0	–	V_{DD} + 0.6	

DC Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		–	–	±10	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = 0V, I_{OUT} = 0mA	f = 8.3MHz	–	–	60	mA
			f = 10MHz	–	–	70	
I_{DDO2}			f = 1MHz	–	–	30	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	1	
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V		–	–	100	μA
V_{OH}	Output High Voltage	I_{OH} = -400μA		2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		–	–	0.4	
I_{PP1}	V_{PP} Current	V_{PP} = 0V ~ V_{DD} + 0.6V		–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{DD}		–	–	±10	

AC Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	TC574096D-10		TC574096D-120		TC574096D-150		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	100	–	120	–	150	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	100	–	120	–	150	
t_{OE}	$\overline{OE}$ to Output Valid	–	50	–	60	–	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	–	50	–	50	–	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	–	50	–	50	–	60	
t_{OH}	Output Data Hold Time	0	–	0	–	0	–	

AC Test Conditions

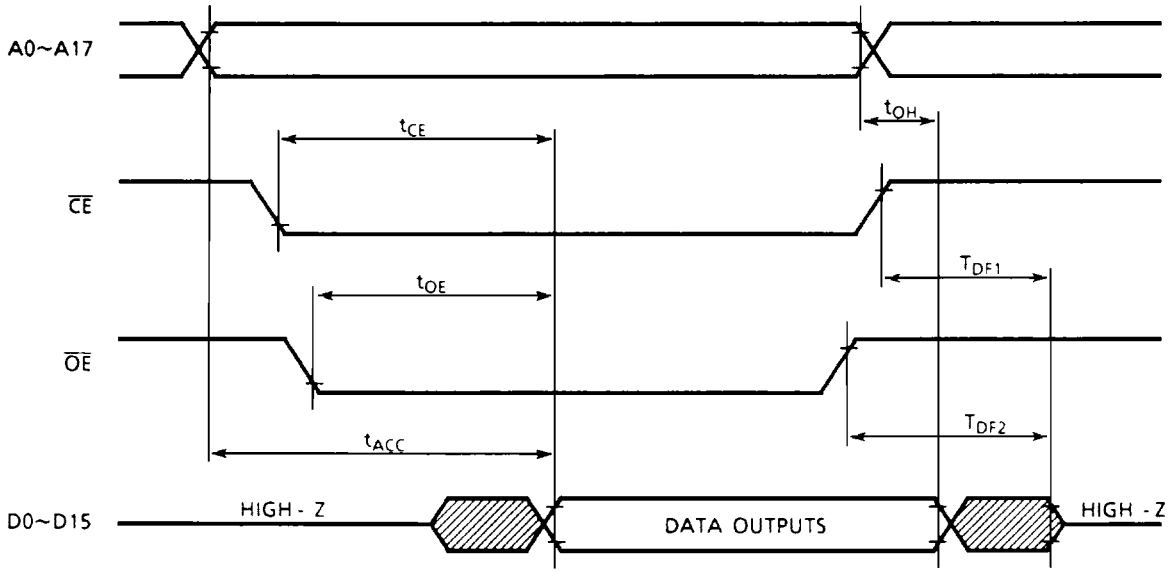
Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	10	12	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms (Read)



High Speed Programming Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 1.0	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	Program Supply Voltage	12.20	12.50	12.80	

DC Characteristics (Ta = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.50V±0.30V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	
I_{DD}	V_{DD} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 12.8V	–	–	50	

AC Programming Characteristics (Ta = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.50V±0.30V)

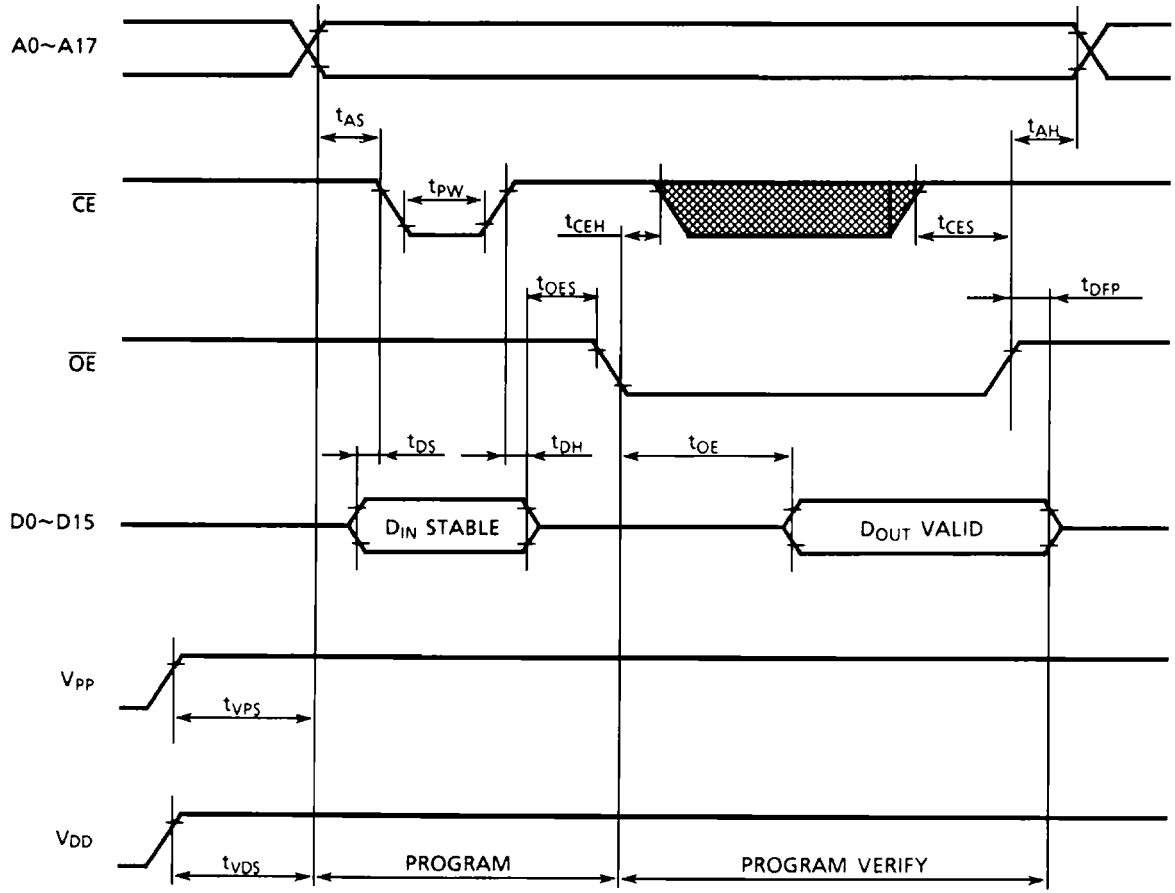
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	2	–	–	
t_{VPS}	V_{PP} Setup Time	–	2	–	–	
t_{VDS}	V_{DD} Setup Time	–	2	–	–	
t_{PW}	Program Pulse Width	–	45	50	55	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IH}	–	–	100	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IH}	–	–	90	

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Timing Waveforms (Program)

High Speed Programming Mode



Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from a programming socket and replacing the device in the socket while V_{PP} = 12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Erasure Characteristics Mode

Erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity [W/cm^2] x exposure time [sec.]) necessary for erasure should be a minimum of 15 [W • sec/cm^2].

When the Toshiba sterilizing lamp (GL-15) is used and the device is exposed at a distance of 1 cm from the lamp surface, erasure will be achieved within 60 minutes. Using commercial lamps whose ultraviolet light intensity is 12000 [μW/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm^2] x (20 x 60) [sec] ≅ 15 [W • sec/cm^2].)

Erasure begins to occur when exposed to light with a wavelength shorter than 4000Å. Sunlight and fluorescent lights have 3000 ~ 4000Å wavelength components. Therefore, when used under these lighting conditions for extended periods of time, opaque seals should be used (Toshiba EPROM Protect Seal AC906).

Operation Information

The TC574096D's six operating modes are listed in the following table.

Mode selection is achieved by applying TTL level signals to appropriate inputs.

MODE \ PIN NAMES		$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D0 ~ D15	POWER
Read Operation (Ta = 0 ~ 70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*				Standby
Program Operation (Ta = 25±5°C)	Program	L	H	12.50V	6.25V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Notes: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Read Mode

The TC574096D has two control inputs. The chip enable ($\overline{CE}$) input controls the operating power and should be used for device selection while the output enable ($\overline{OE}$) input controls the output buffers. Assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL}, once the address has stabilized, output data will be valid after the address access time has elapsed. The $\overline{CE}$ to output valid time (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$ = V_{IL} and that the address has been stable for at least t_{ACC}, then output data will be valid after t_{OE} from the falling edge of $\overline{OE}$.

Output Deselect Mode

If $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, the outputs will be in a high impedance state.

Therefore, two or more devices can be connected together on a common bus if the output of only one device is enabled. When $\overline{CE}$ is used for device selection, all deselected devices are in the low power standby mode.

Standby Mode

The TC574096D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a MOS high level voltage (V_{DD}) to the $\overline{CE}$ input, the TC574096D is placed in the standby mode which reduces the operating current to 100μA and puts the outputs in a high impedance state, independent of the $\overline{OE}$ input.

Program Mode

When the TC574096D is initially received by customers, all bits of the device are in the "1" state, which is the erased state. Therefore, the object of the program operation is to introduce "0" data into the desired bit locations. The TC574096D is in the programming mode when V_{PP} = 12.5V, $\overline{CE}$ = V_{IL}, and $\overline{OE}$ = V_{IH}.

The TC574096D can be programmed at any address location at any time - either individually, sequentially, or at random.

Program Verify Mode

The verify mode is used to check that the desired data has been correctly programmed. The verify mode is activated when $\overline{OE}$ = V_{IL}.

Program Inhibit Mode

When the programming voltage (+12.5V) is applied to the V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC574096D from

being programmed.

The programming of two or more TC574096Ds in parallel with different data is easily accomplished. All inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, then a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only while a TTL high level signal is applied to the $\overline{CE}$ of the other devices.

High Speed Programming Mode

The device is set up in high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{DD} = 6.25V.

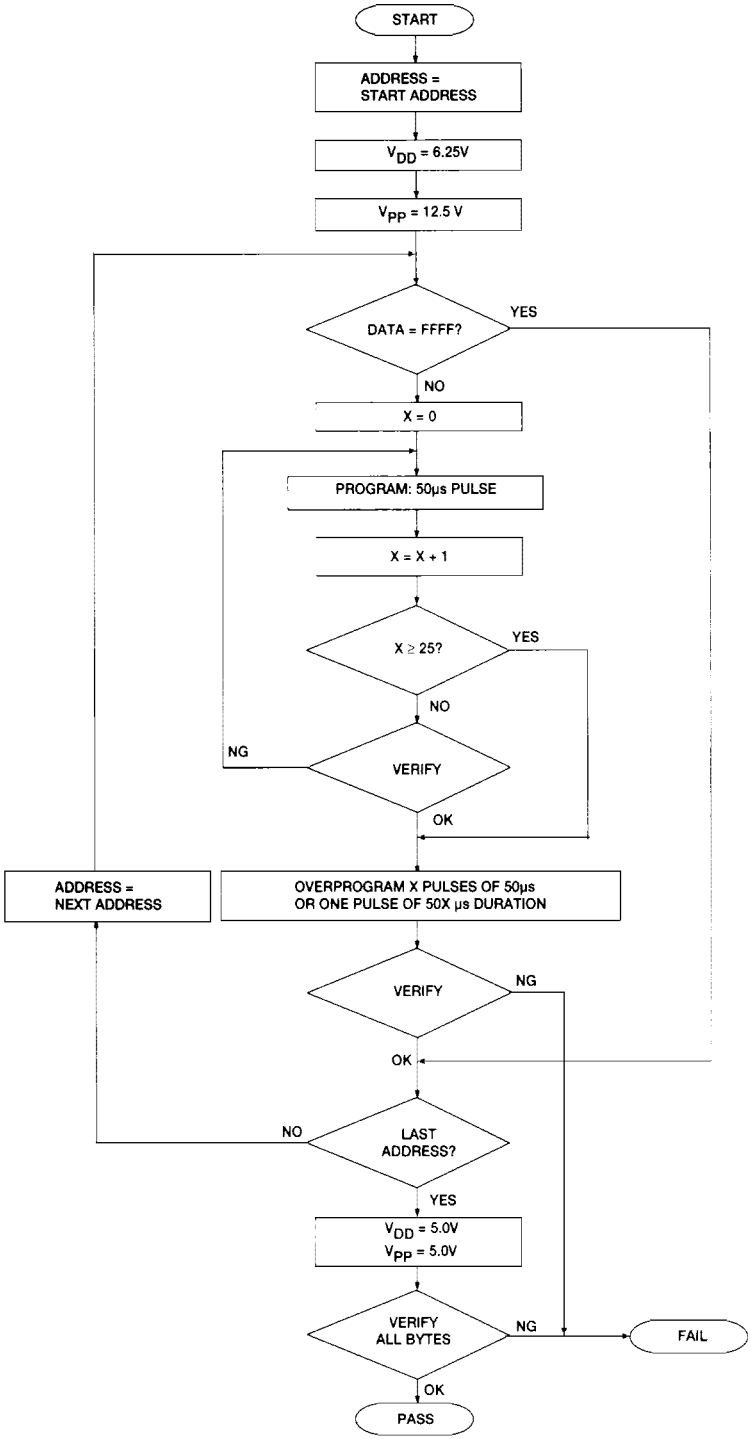
Programming is achieved by applying a single 50μs TTL low level pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using the program verify mode. If the programmed data is not correct, another program pulse of 50μs is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

After correctly programming the selected address, an overprogram pulse with the same width as that needed for initial programming should be applied.

When programming has been completed, the data in all addresses should be verified with $V_{DD} = V_{PP} = 5V$.

High Speed Programming Mode

Flow Chart



Electric Signature Mode

The electric signature mode allows one to read out a code from the TC574096D which identifies its manufacturer and device type.

The programming equipment may read out the manufacturer code and device code from the TC574096D by using this mode before programming and automatically set the programming voltage (V_{PP}) and algorithm.

The electric signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} during a read operation. Data output under these conditions is the manufacturer code. The device code is output when address A0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit being (D7). The following table shows the electric signature of the TC574096D.

PINS / SIGNATURE	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX. DATA
Manufacturer Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	0	0	0	0	1	1	1	0	**0E

Notes: A9 = 12V±0.5V
A1 ~ A8, A10 ~ A17, $\overline{CE}$, $\overline{OE}$ = V_{IL}

* Don't care