

Am2954 • Am2955

Octal Registers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Am2954 has non-inverting inputs
- Am2955 has inverting inputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- $V_{OL} = 0.5V$ (max) at $I_{OL} = 32mA$
- High-speed - Clock to output 11ns typical

FUNCTIONAL DESCRIPTION

The Am2954 and Am2955 are 8-bit registers built using high-speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the 3-state condition.

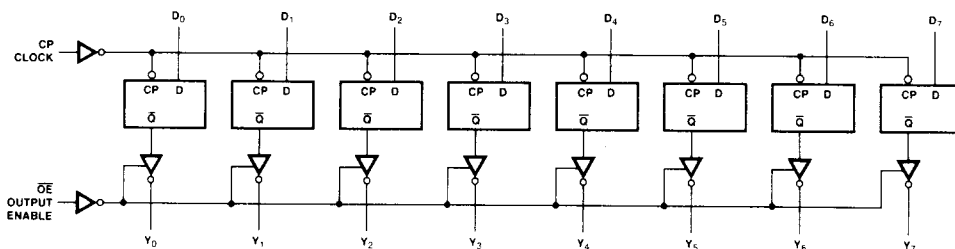
Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

RELATED PRODUCTS

Part No.	Description
Am29821-26	8, 9, 10-Bit Registers
Am2918	Quad D-Register
Am2920	Quad D-Type Flip-Flop

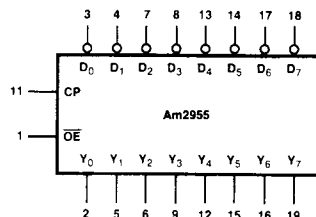
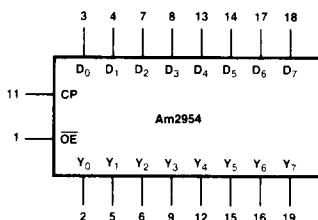
LOGIC DIAGRAM Am2954



Inputs D_0 through D_7 are inverted on the Am2955.

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LOGIC SYMBOLS

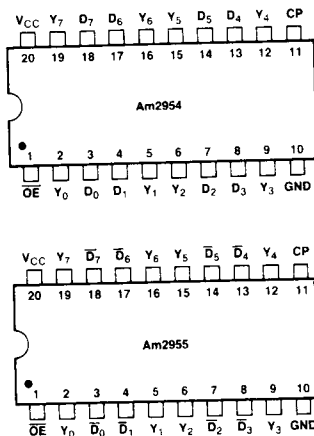
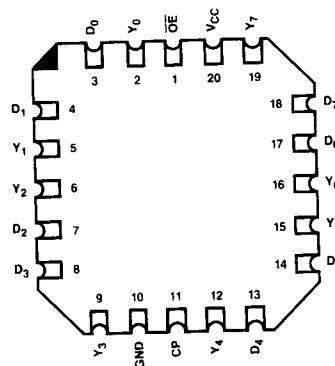


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V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAMS Top Views

D-20, P-20

Leadless Chip Carrier
L-20-1

F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am2954 Order Number	Am2955 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2954PC	AM2955PC	P-20	C	C-1
AM2954DC	AM2955DC	D-20	C	C-1
AM2954DC-B	AM2955DC-B	D-20	C	B-1
AM2954DM	AM2955DM	D-20	M	C-3
AM2954DM-B	AM2955DM-B	D-20	M	B-3
AM2954FM	AM2955FM	F-20	M	C-3
AM2954FM-B	AM2955FM-B	F-20	M	B-3
AM2954LC	AM2955LC	L-20-1	C	C-1
AM2954LC-B	AM2955LC-B	L-20-1	C	B-1
AM2954LM	AM2955LM	L-20-1	M	C-3
AM2954LM-B	AM2955LM-B	L-20-1	M	B-3
AM2954XC	AM2955XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2954XM	AM2955XM	Dice	M	

- Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = -55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-3 conform to MIL-STD-883, Class B.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2954XC, DC, PC	Am2955XC, DC, PC	$T_A = 0 \text{ to } 70^\circ\text{C}$	$V_{CC} = 4.75 \text{ to } 5.25\text{V}$
Am2954XM, DM, FM	Am2955XM, DM, FM	$T_C = -55 \text{ to } +125^\circ\text{C}$	$V_{CC} = 4.50 \text{ to } 5.50\text{V}$

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	MIL, $I_{OH} = -2.0\text{mA}$	2.4	3.4	Volts
			COM'L, $I_{OH} = -6.5\text{mA}$	2.4	3.1	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\text{mA}$		.45	Volts
			$I_{OL} = 32\text{mA}$		.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	$V_{CC} = \text{MIN}$, $I_{IN} = -18\text{mA}$			-1.2	Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5\text{V}$			-250	μA
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7\text{V}$			50	μA
I_I	Input HIGH Current	$V_{CC} = \text{MAX}$, $V_{IN} = 5.5\text{V}$			1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	$V_{CC} = \text{MAX}$	$V_O = 0.5\text{V}$		-50	μA
			$V_O = 2.4\text{V}$		50	
I_{SC}	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC}	Power Supply Current (Note 4)	$V_{CC} = \text{MAX}$		90	140	mA

- Notes: 1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. Am2954 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.
 Am2955 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 to +150°C
Temperature (Ambient) Under Bias	-55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	-0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	-0.5V to + V_{CC} max
DC Input Voltage	-0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	-30 to +5.0mA

DEFINITION OF FUNCTIONAL TERMS D_i The D flip-flop data inputs (Am2954, non-inverting). $\overline{D}_i$ The D flip-flop data inputs (Am2955, inverting).**CP** Clock Pulse for the register. Enters data on the LOW-to-HIGH transition. Y_i The register three-state outputs (Am2954, non-inverting). **$\overline{OE}$** Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.**FUNCTION TABLE**

Function	Inputs				Internal	Outputs
	$\overline{OE}$	Clock	Am2954 D_i	Am2955 $\overline{D}_i$	Q_i	Y_i
Hi-Z	H	L	X	X	NC	Z
	H	H	X	X	NC	Z
LOAD REGISTER	L	↑	L	H	L	L
	L	↑	H	L	H	H
	H	↑	L	H	L	Z
	H	↑	H	L	H	Z

H = HIGH

NC = No Change

L = LOW

Z = High Impedance

X = Don't Care

↑ = LOW-to-HIGH transition

SWITCHING CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5.0V)

		Am2954 • Am2955			Units	Test Conditions
Parameters	Description	Min	Typ	Max		
t _{PLH}	Clock to Output, Y _i		8	15	ns	C _L = 15pF R _L = 280Ω
t _{PHL}			11	17	ns	
t _{ZH}	$\overline{OE}$ to Y _i		8	15	ns	
t _{ZL}			11	18	ns	
t _{HZ}	$\overline{OE}$ to Y _i		5	9	ns	C _L = 5pF R _L = 280Ω
t _{LZ}			7	12	ns	
t _{pw}	Clock Pulse Width	HIGH	6		ns	C _L = 15pF R _L = 280Ω
		LOW	7.3		ns	
t _S	Data to Clock	5			ns	
t _H		2			ns	
f _{max}	Maximum Clock Frequency (Note 1)	75	100		MHz	

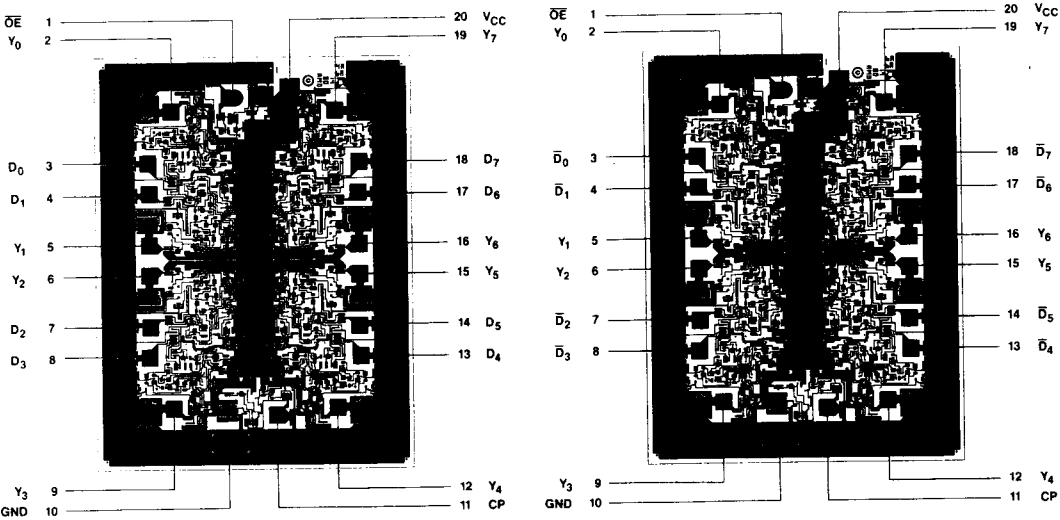
Note: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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METALLIZATION AND PAD LAYOUTS

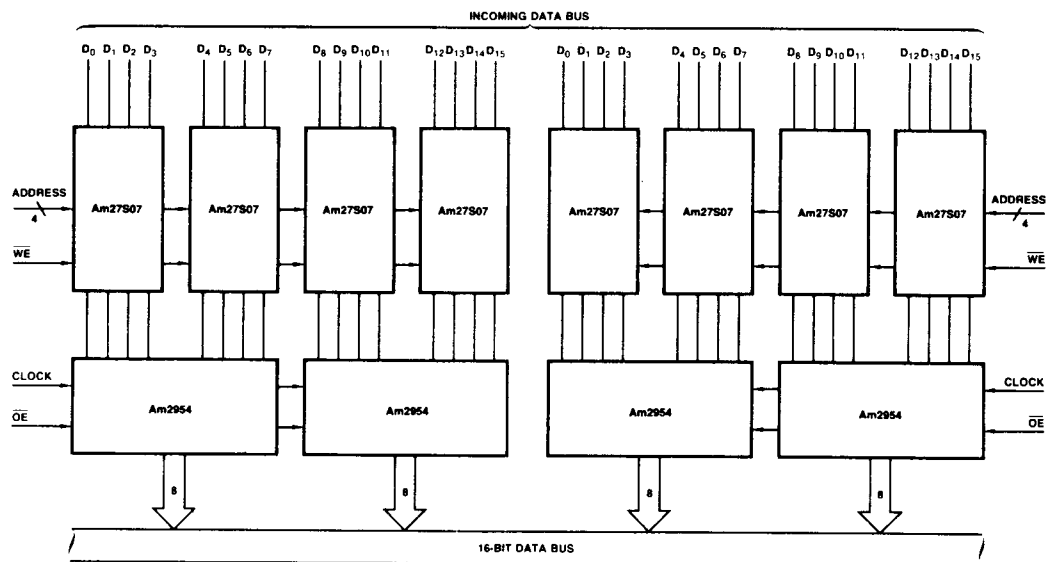
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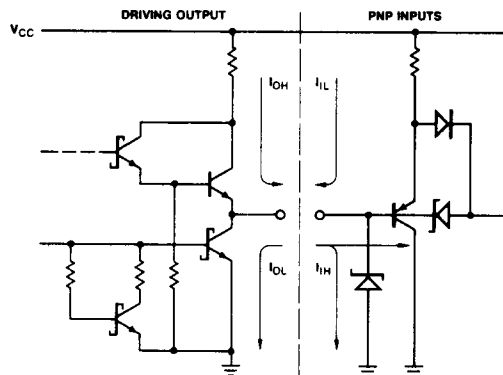
DIE SIZE 0.085" X 0.110"

APPLICATION



Dual 16-word by 16-bit non-inverting high-speed data buffer.

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SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS

Note: Actual current flow direction shown.

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