

**SN54251, SN54LS251 SN54S251,
SN74251, SN74LS251, (TIM9905), SN74S251
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS**

SDLS085 – DECEMBER 1972 – REVISED MARCH 1988

- Three-State Versions of '151, 'LS151, 'S151
- Three-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Permit Multiplexing from N-lines to One Line
- Complementary Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL Circuits

TYPE	MAX NO. OF COMMON OUTPUTS	TYPICAL AVG PROP	TYPICAL
		DELAY TIME (D TO Y)	POWER DISSIPATION
SN54251	49	17 ns	250 mW
SN74251	129	17 ns	250 mW
SN54LS251	49	17 ns	35 mW
SN74LS251	129	17 ns	35 mW
SN54S251	39	8 ns	275 mW
SN74S251	129	8 ns	275 mW

description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

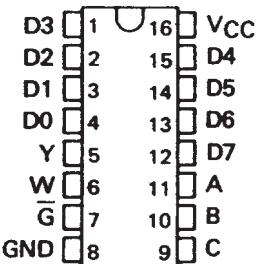
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time. The SN54251 and SN74251 have output clamp diodes to attenuate reflections on the bus line.

SN54251, SN54LS251, SN54S251 . . . J OR W PACKAGE

SN74251 . . . N PACKAGE

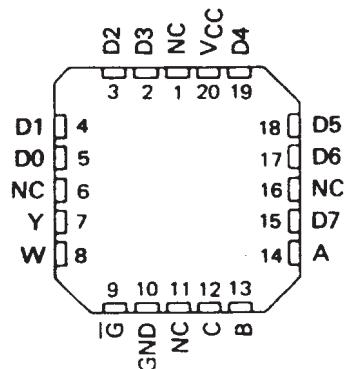
SN74LS251, SN74S251 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS251, SN54S251 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS	
SELECT	ENABLE	G	Y	W
C	B	A	Z	Z
X	X	X	H	Z
L	L	L	L	$\overline{D_0}$
L	L	H	L	$\overline{D_1}$
L	H	L	L	$\overline{D_2}$
L	H	H	L	$\overline{D_3}$
H	L	L	L	$\overline{D_4}$
H	L	H	L	$\overline{D_5}$
H	H	L	L	$\overline{D_6}$
H	H	H	L	$\overline{D_7}$

H = high logic level, L = low logic level

X = irrelevant, Z = high impedance (off)

D0, D1 . . . D7 = the level of the respective D input

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

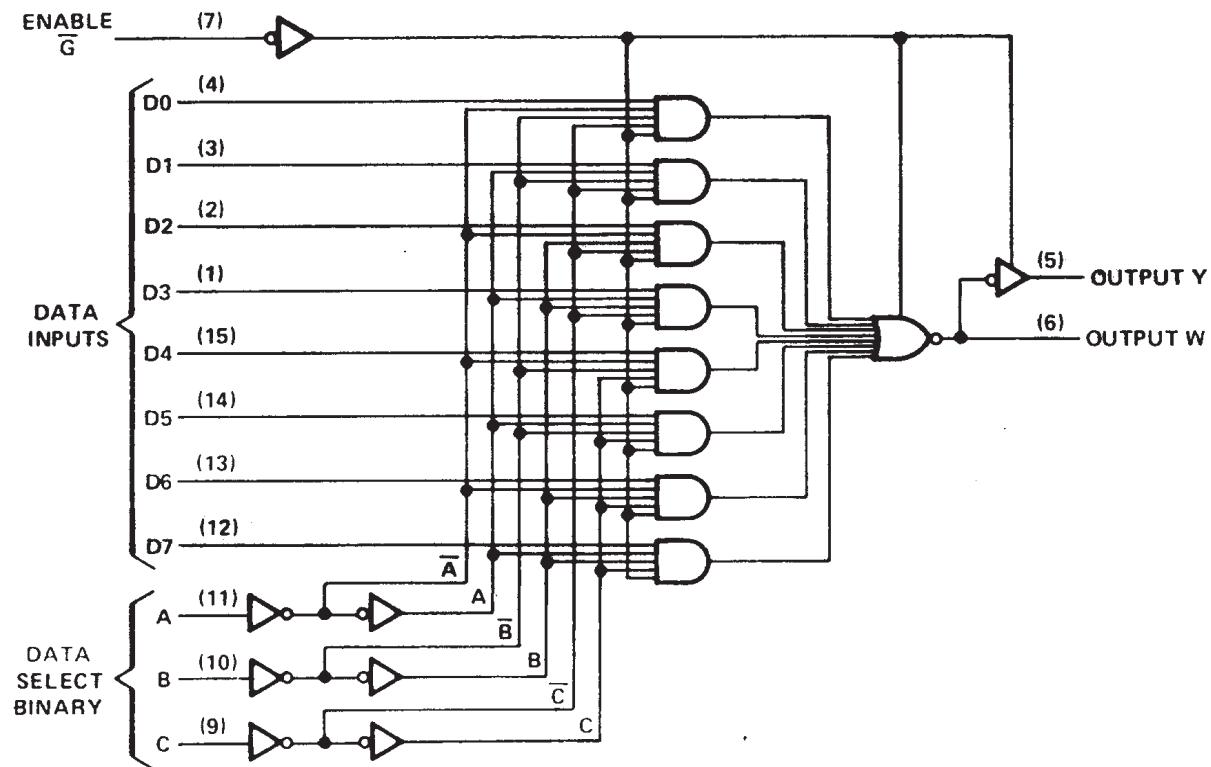
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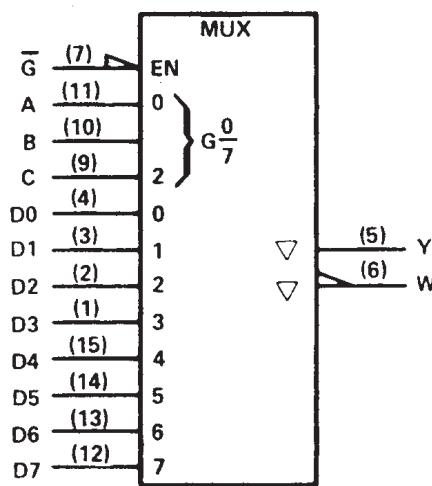
**SN54251, SN54LS251 SN54S251,
SN74251, SN74LS251, (TIM9905), SN74S251
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS**

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logic diagram (positive logic)



logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN54251 SN74251, DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54251			SN74251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-5.2	mA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55	125	0	0	70	0	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage			0.8		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = \text{MAX}$	2.4	3.2		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.2	0.4
I_{OZ}	Off-state (high-impedance-state) output current	$V_{CC} = \text{MAX}$,	$V_O = 2.4 \text{ V}$	40		μA
		$V_{IH} = 2 \text{ V}$	$V_O = 0.4 \text{ V}$	-40		
V_O	Output clamp voltage	$V_{CC} = \text{MAX}$,	$I_O = -12 \text{ mA}$	-1.5		V
		$V_{IH} = 4.5 \text{ V}$	$I_O = 12 \text{ mA}$	$V_{CC} + 1.5$		
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$			-18	-55
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, All inputs at 4.5 V, All outputs open			38	62
						mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

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switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	$C_L = 50 \text{ pF}$, $R_L = 400 \Omega$, See Note 2	29	45		ns
t_{PHL}				28	45		
t_{PLH}				20	33		
t_{PHL}				21	33		
t_{PLH}				17	28		
t_{PHL}				18	28		
t_{PLH}				10	15		
t_{PHL}				9	15		
t_{PZH}				17	27		
t_{PZL}				26	40		
t_{PZH}	\bar{G}	Y	$C_L = 5 \text{ pF}$, $R_L = 400 \Omega$, See Note 2	17	27		ns
t_{PZL}				24	40		
t_{PHZ}				5	8		ns
t_{PLZ}				15	23		
t_{PHZ}	\bar{G}	W	$C_L = 5 \text{ pF}$, $R_L = 400 \Omega$, See Note 2	5	8		ns
t_{PLZ}				15	23		

[†] t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

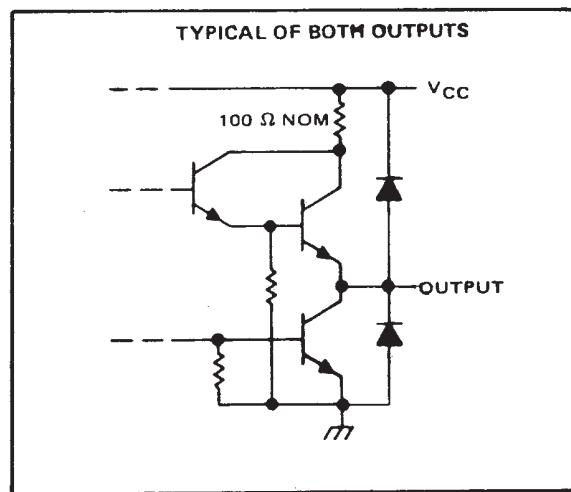
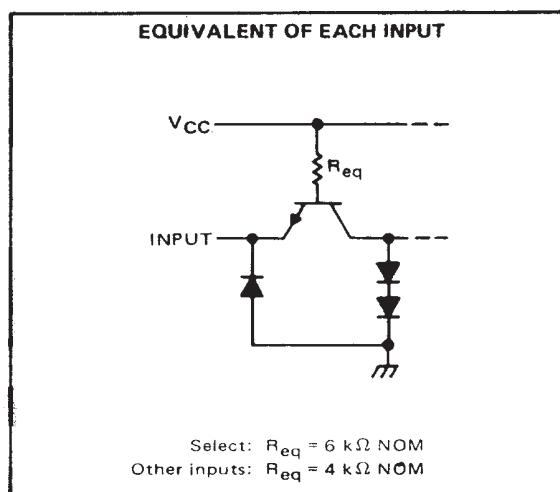
t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

t_{PLZ} = Output disable time from low level

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



SN54LS251 SN74LS251, DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS251	55°C to 125°C
SN74LS251	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS251			SN74LS251			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS251			SN74LS251			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$ $I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.1		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 8 \text{ mA}$			0.35	0.5		
I_{OZ}	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$	$V_O = 2.7 \text{ V}$	20		20			μA
		$V_O = 0.4 \text{ V}$		-20		-20		
I_I	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.1		0.1		0.1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		20		20		20	μA
I_{IL}	$\text{Enable } \bar{G}$ All other	$V_{CC} = \text{MAX}$, $V_I = 0.4$		-0.2		-0.2		mA
				-0.4		-0.4		
$I_{OS\$}$	$V_{CC} = \text{MAX}$	-30	-130		-30	-130		mA
I_{CC}	$V_{CC} = \text{MAX}$, See Note 3	Condition A	6.1	10	6.1	10		mA
		Condition B	7.1	12	7.1	12		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with the outputs open and all data and select inputs at 4.5 V under the following conditions:

- A. Enable grounded.
- B. Strobe at 4.5 V.

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switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 2	29	45		ns
t_{PHL}				28	45		ns
t_{PLH}				20	33		ns
t_{PHL}				21	33		ns
t_{PLH}				17	28		ns
t_{PHL}				18	28		ns
t_{PLH}				10	15		ns
t_{PHL}				9	15		ns
t_{PZH}				30	45		ns
t_{PZL}				26	40		ns
t_{PZH}				17	27		ns
t_{PZL}				24	40		ns
t_{PHZ}	\bar{G}	Y	$C_L = 5 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 2	30	45		ns
t_{PLZ}				15	25		ns
t_{PHZ}				37	55		ns
t_{PLZ}				15	25		ns

[†] t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

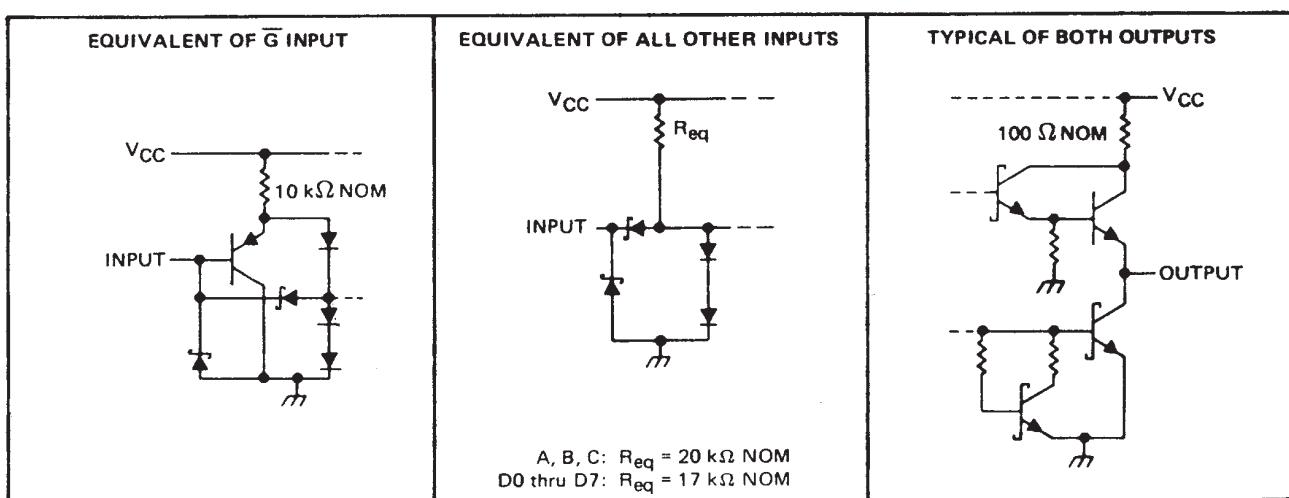
t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

t_{PLZ} = Output disable time from low level

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



SN54S251 SN74S251, DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S251			SN74S251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-6.5	mA
Low-level output current, I_{OL}				20		20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]			MIN	TYP [‡]	MAX	UNIT
V _{IH}	High-level input voltage				2			V
V _{IL}	Low-level input voltage						0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA					-1.2	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V,	SN54S'	2.4	3.4		V
		I _{OH} = MAX		SN74S'	2.4	3.2		
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V,				0.5	V
		I _{OL} = 20 mA						
I _{OZ}	Off-state (high-impedance-state) output current	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.4 V		50			μA
			V _O = 0.5 V				-50	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V				1		mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V				50		μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5 V				-2		mA
I _{OS}	Short-circuit output current [§]	V _{CC} = MAX			-40	-100		mA
I _{CC}	Supply current	V _{CC} = MAX, All inputs at 4.5 V,					55	mA
		All outputs open					85	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[†]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54S251 SN74S251, DATA SELECTORS/MUXES WITH 3-STATE OUTPUTS

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switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	$C_L = 15 \text{ pF}$, $R_L = 280 \Omega$, See Note 2	12	18		ns
t_{PHL}	A, B, or C (3 levels)	W		13	19.5		
t_{PLH}	Any D	Y		10	15		ns
t_{PHL}	Any D	W		9	13.5		
t_{PLH}	Any D	Y		8	12		ns
t_{PHL}	Any D	W		8	12		
t_{PLH}	—	Y		4.5	7		ns
t_{PHL}	—	W		4.5	7		
t_{PZH}	\bar{G}	Y		13	19.5		ns
t_{PZL}	\bar{G}	W		14	21		
t_{PZH}	\bar{G}	Y	$C_L = 50 \text{ pF}$, $R_L = 280 \Omega$, See Note 2	13	19.5		ns
t_{PZL}	\bar{G}	W		14	21		
t_{PHZ}	\bar{G}	Y		5.5	8.5		ns
t_{PLZ}	\bar{G}	W		9	14		
t_{PHZ}	\bar{G}	Y	$C_L = 5 \text{ pF}$, $R_L = 280 \Omega$, See Note 2	5.5	8.5		ns
t_{PLZ}	\bar{G}	W		9	14		

[†] t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

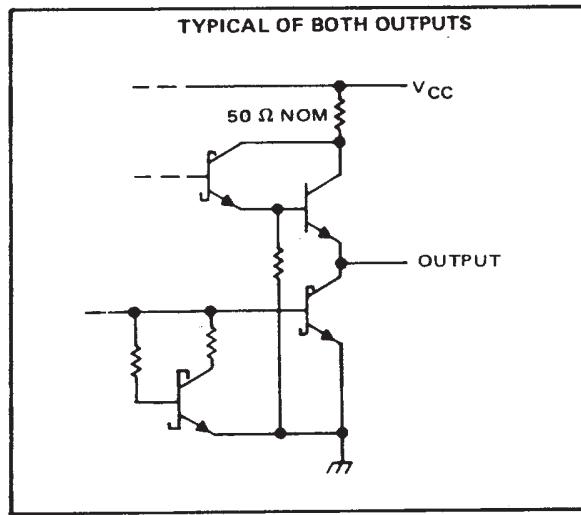
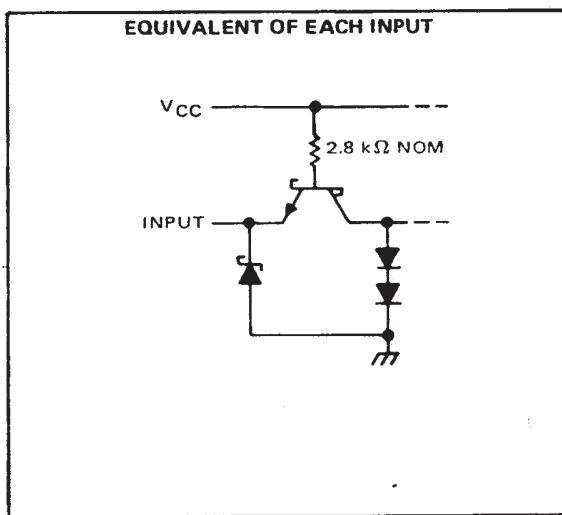
t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

t_{PLZ} = Output disable time from low level

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7601601EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7601601EA SNJ54LS251J	Samples
7601601FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7601601FA SNJ54LS251W	Samples
7601601FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7601601FA SNJ54LS251W	Samples
JM38510/30905BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30905BEA	Samples
JM38510/30905BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30905BEA	Samples
M38510/30905BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30905BEA	Samples
M38510/30905BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 30905BEA	Samples
SN54LS251J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS251J	Samples
SN54LS251J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS251J	Samples
SN74LS251D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS251	Samples
SN74LS251D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS251	Samples
SN74LS251DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS251	Samples
SN74LS251DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS251	Samples
SN74LS251N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS251N	Samples
SN74LS251N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS251N	Samples
SN74LS251NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS251N	Samples
SN74LS251NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS251N	Samples
SN74LS251NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS251	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS251NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS251	Samples
SNJ54LS251FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 251FK	Samples
SNJ54LS251FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 251FK	Samples
SNJ54LS251J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7601601EA SNJ54LS251J	Samples
SNJ54LS251J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7601601EA SNJ54LS251J	Samples
SNJ54LS251W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7601601FA SNJ54LS251W	Samples
SNJ54LS251W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7601601FA SNJ54LS251W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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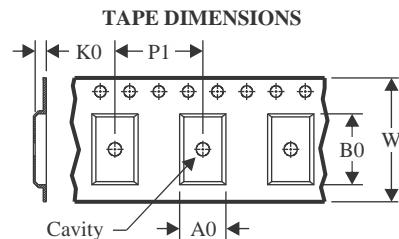
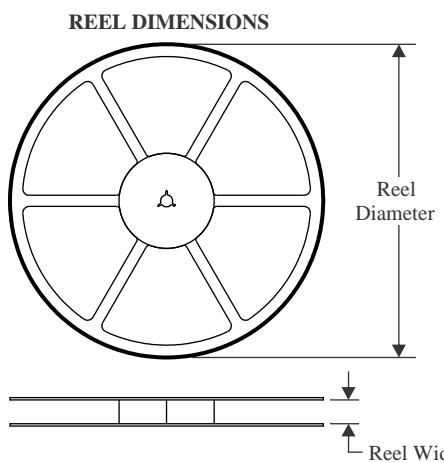
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS251, SN74LS251 :

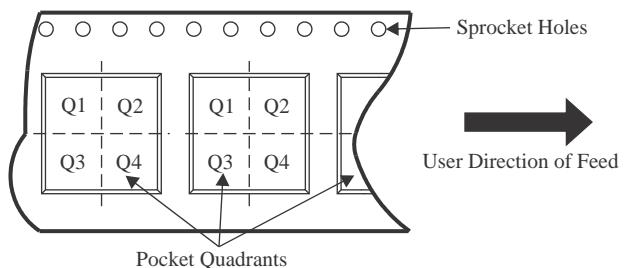
- Catalog : [SN74LS251](#)
- Military : [SN54LS251](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


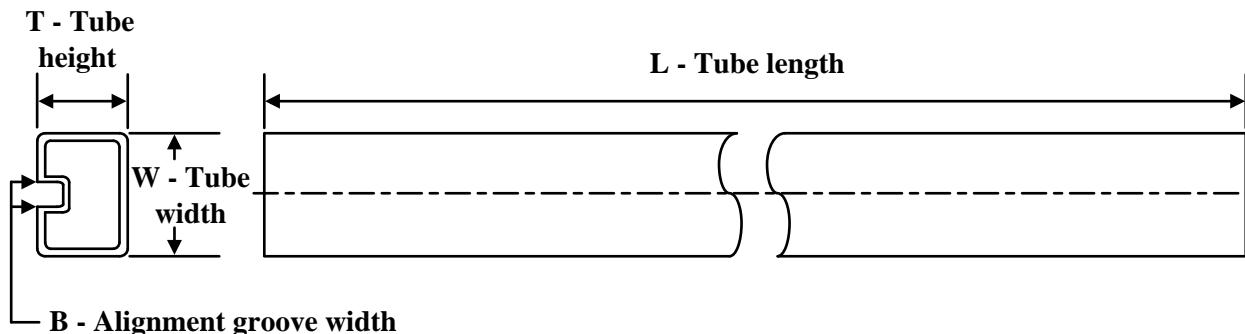
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS251DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS251NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS251DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS251NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE


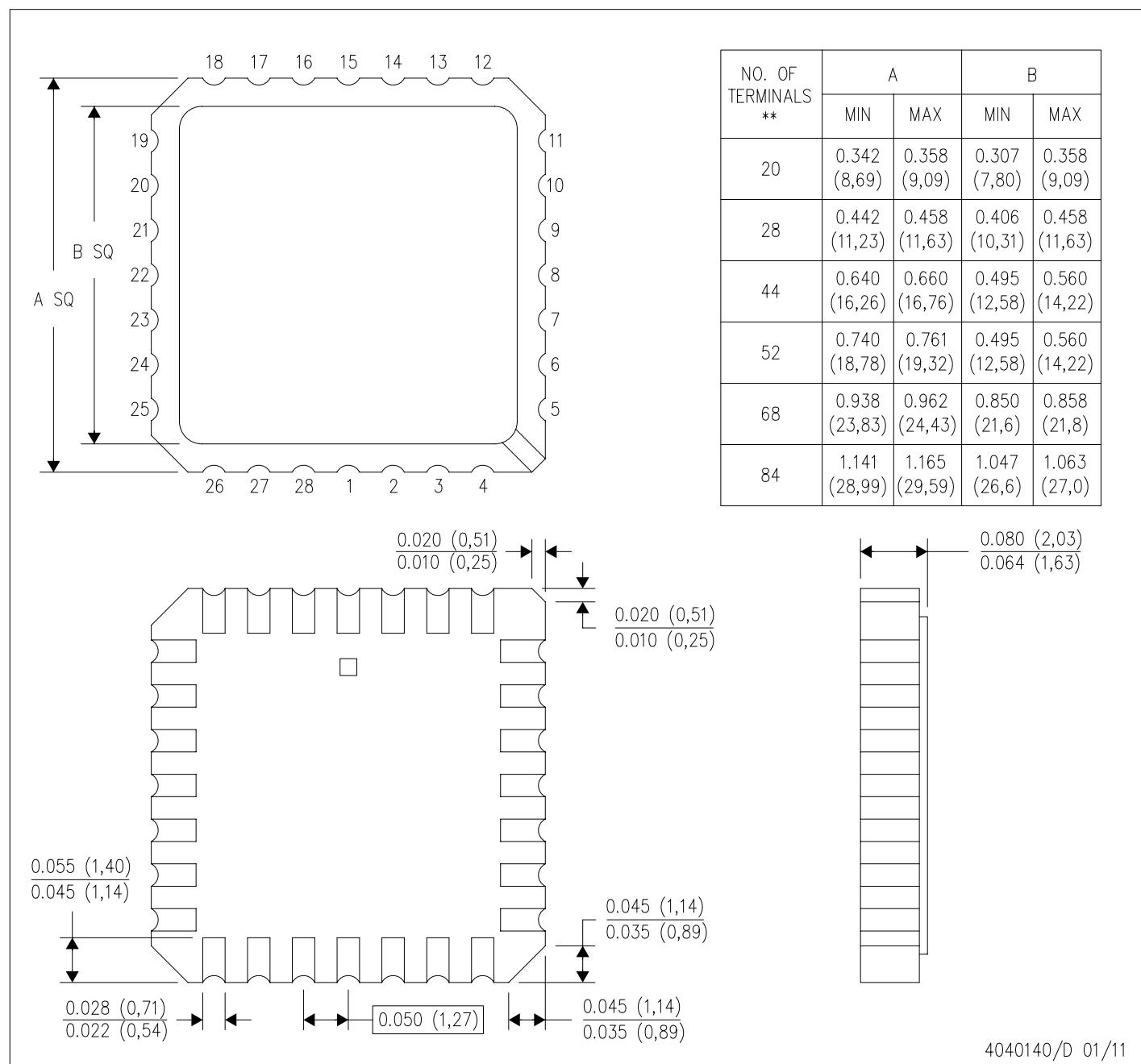
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74LS251D	D	SOIC	16	40	507	8	3940	4.32
SN74LS251N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS251N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS251NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS251NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS251FK	FK	LCCC	20	1	506.98	12.06	2030	NA

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



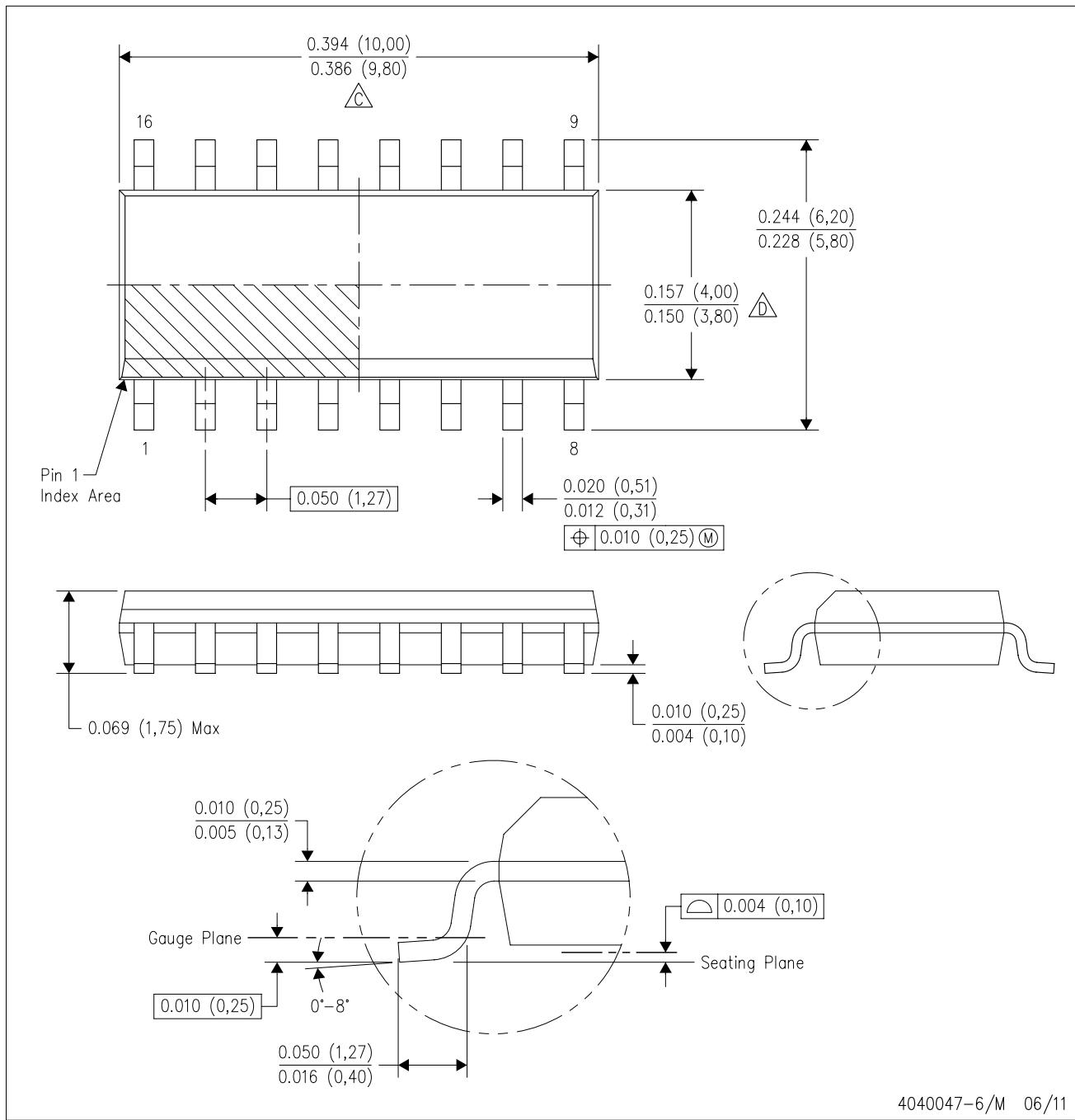
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

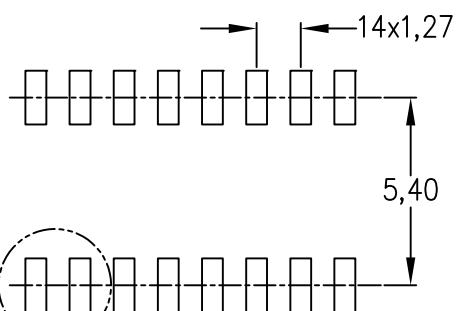
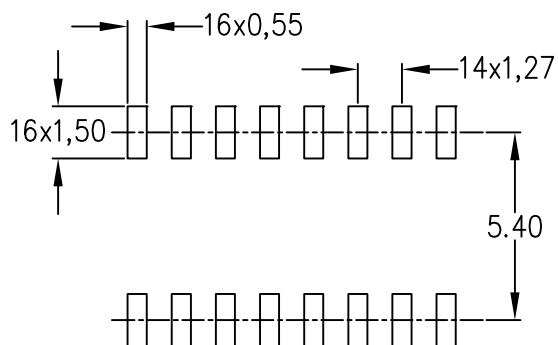
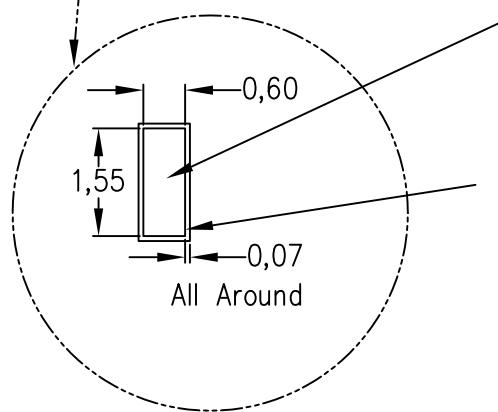
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

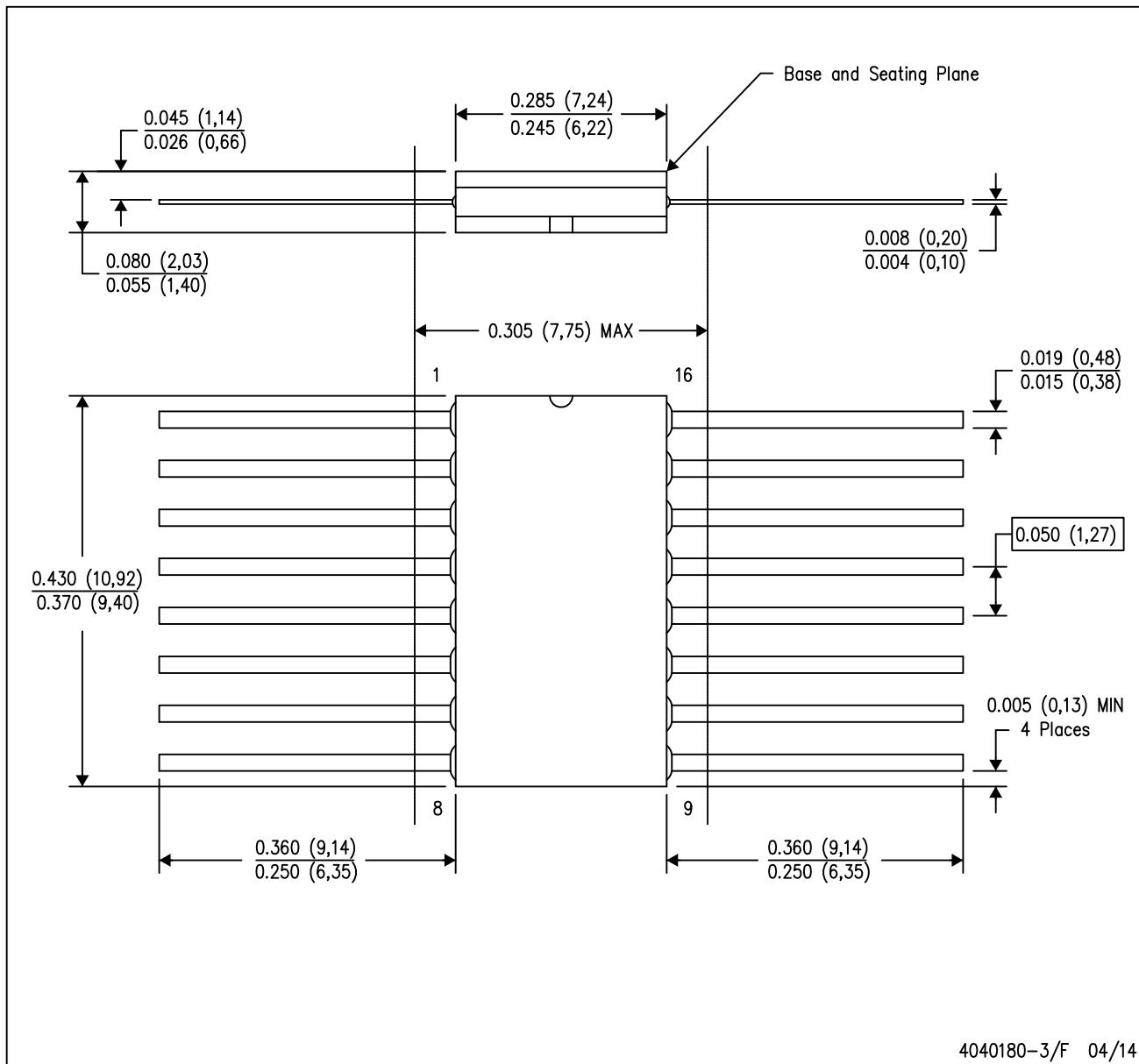


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/F 04/14

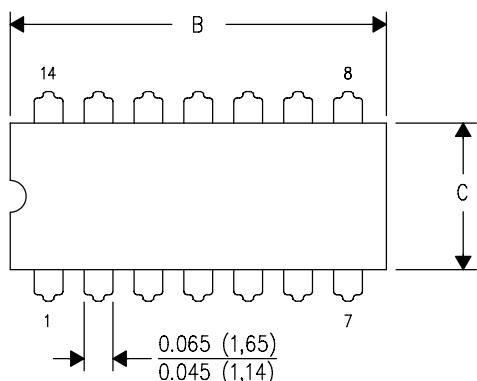
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

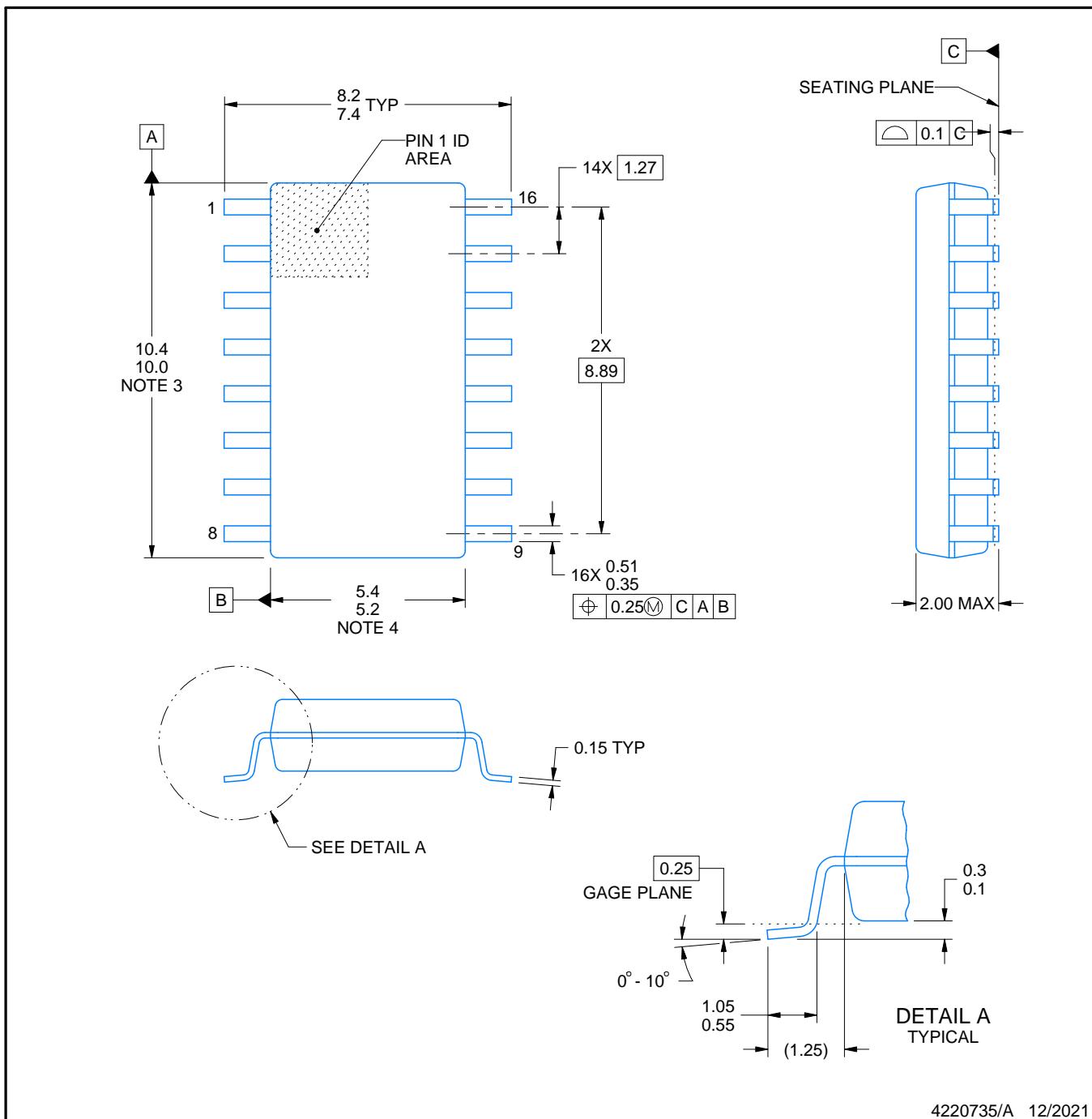
△ The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



NOTES:

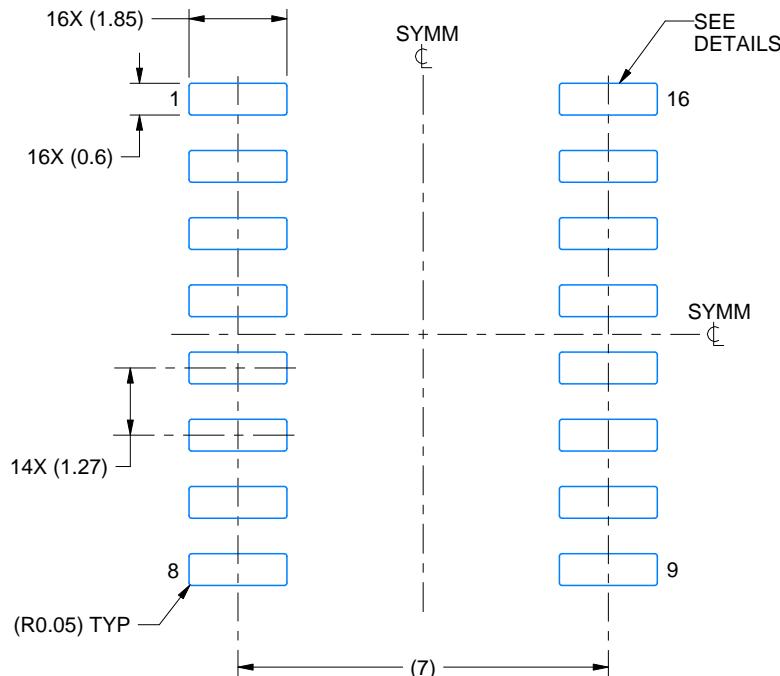
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

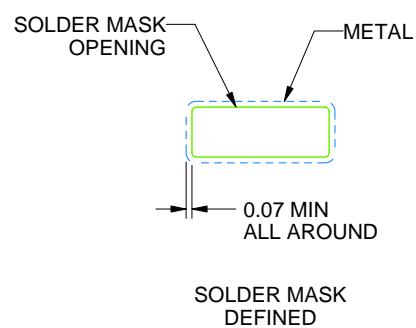
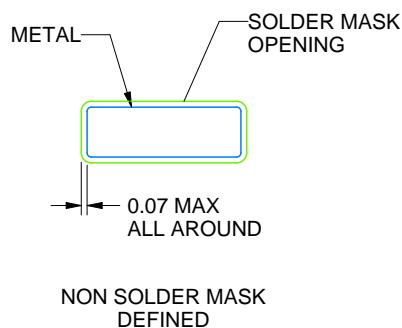
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

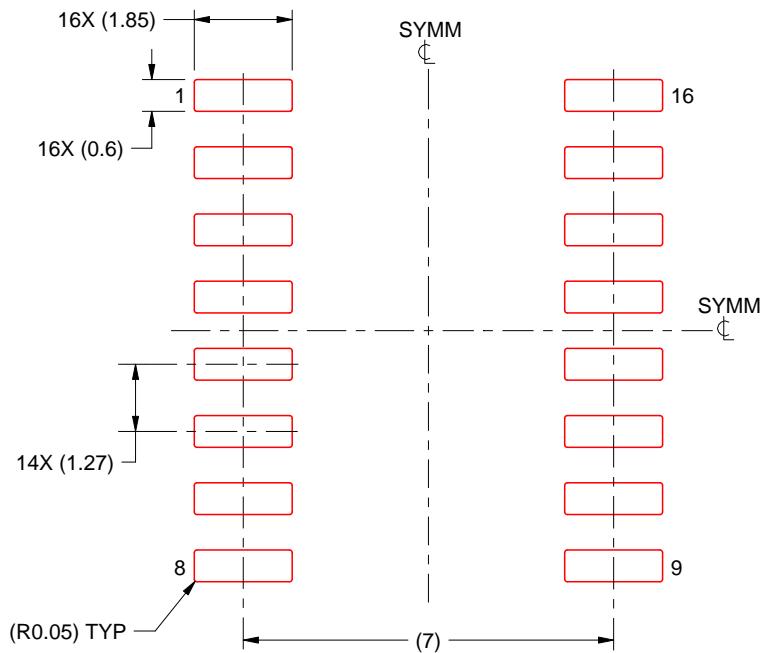
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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