

SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

SDLS091

OCTOBER 1976 — REVISED MARCH 1988

- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Separate Negative-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Typical Clock Input Frequency . . . 50 MHz
- Fully Buffered Outputs

description

These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by up to 50%. They feature hysteresis at each clock input, fully buffered outputs, and direct clear capability, and are presetable through a buffer that also features an input hysteresis loop. The negative-edge-triggering clocks are directly compatible with earlier Series 54/74 single and dual pulse-triggered flip-flops. These circuits can be used to emulate D- or T-type flip-flops by hard-wiring the inputs, or to implement asynchronous sequential functions.

The SN54276 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74276 is characterized for operation from 0°C to 70°C .

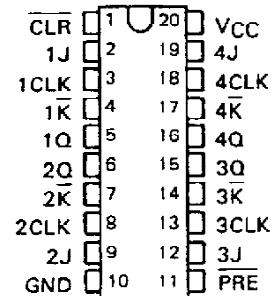
FUNCTION TABLE (EACH FLIP-FLOP)

COMMON INPUTS		INPUTS		OUTPUT	
PRE	CLR	CLK	J	K	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	H [†]
H	H	I	L	H	Q ₀
H	H	I	H	H	H
H	H	I	L	L	L
H	H	I	H	L	TOGGLE
H	H	H	X	X	Q ₀

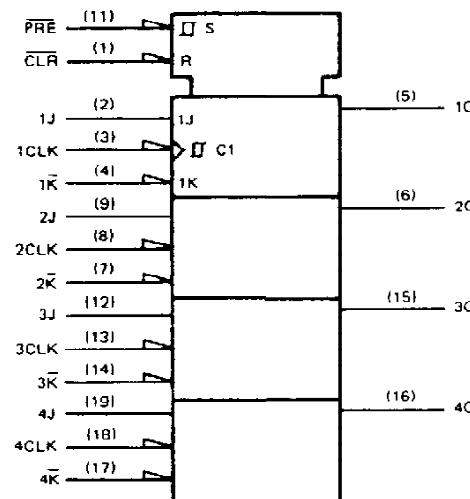
[†] This configuration is nonstable; that is, Q may not persist when preset and clear return to their inactive (high) level.

SN54276 . . . J PACKAGE
SN74276 . . . N PACKAGE

(TOP VIEW)



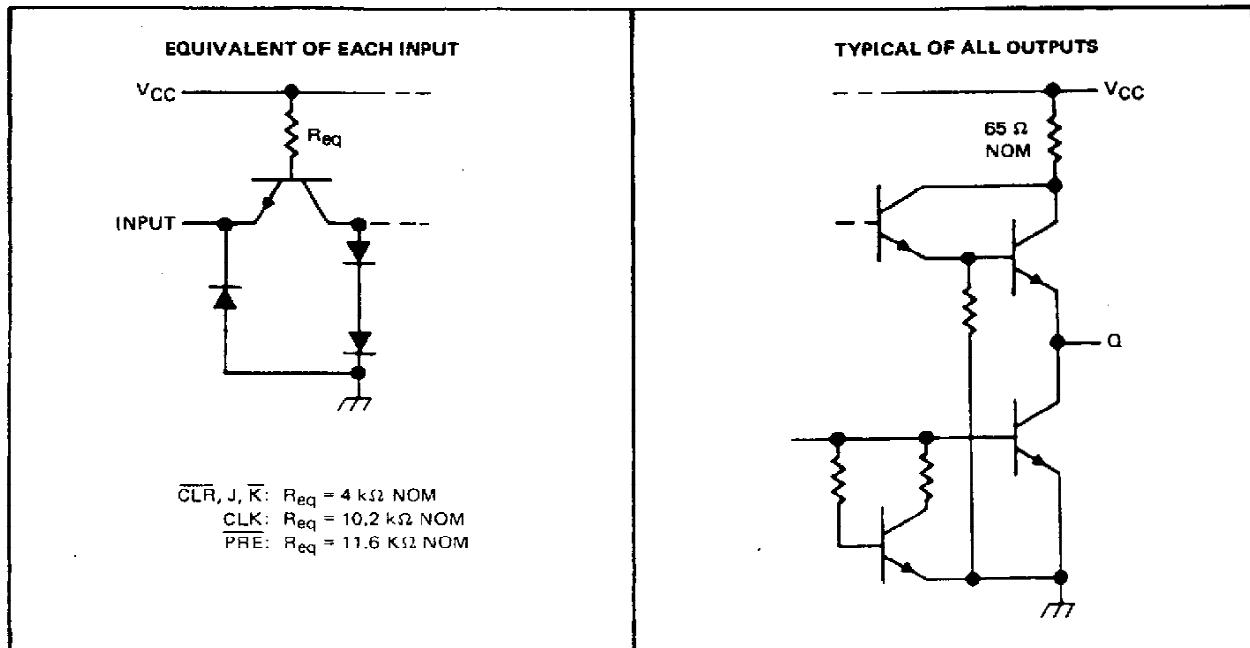
logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN54276, SN74276
QUADRUPLE J-K FLIP-FLOPS**

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

recommended operating conditions

	SN54276			SN74276			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency	0		35	0		35	MHz
Pulse width, t_W	Clock high	13.5		13.5			ns
	Clock low	15		15			
	Preset or clear low	12		12			
Setup time, t_{SU}	J, K inputs	31		34			ns
	Clear and preset inactive state	101		101			
Input hold time, t_h		101		101			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

† The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu A$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-30		-85	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$		60	81	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

[§] Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		35	50		MHz
t_{PLH} Propagation delay time, low-to-high-level output from preset	$C_L = 15 \text{ pF}$		15	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear	$R_L = 400 \Omega$		18	30	ns
t_{PLH} Propagation delay time, low-to-high level output from clock	See Note 2		17	30	ns
t_{PHL} Propagation delay time, high-to-low level output from clock			20	30	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74276DW	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74276DWR	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74276DWR	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74276N	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74276N	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74276N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74276N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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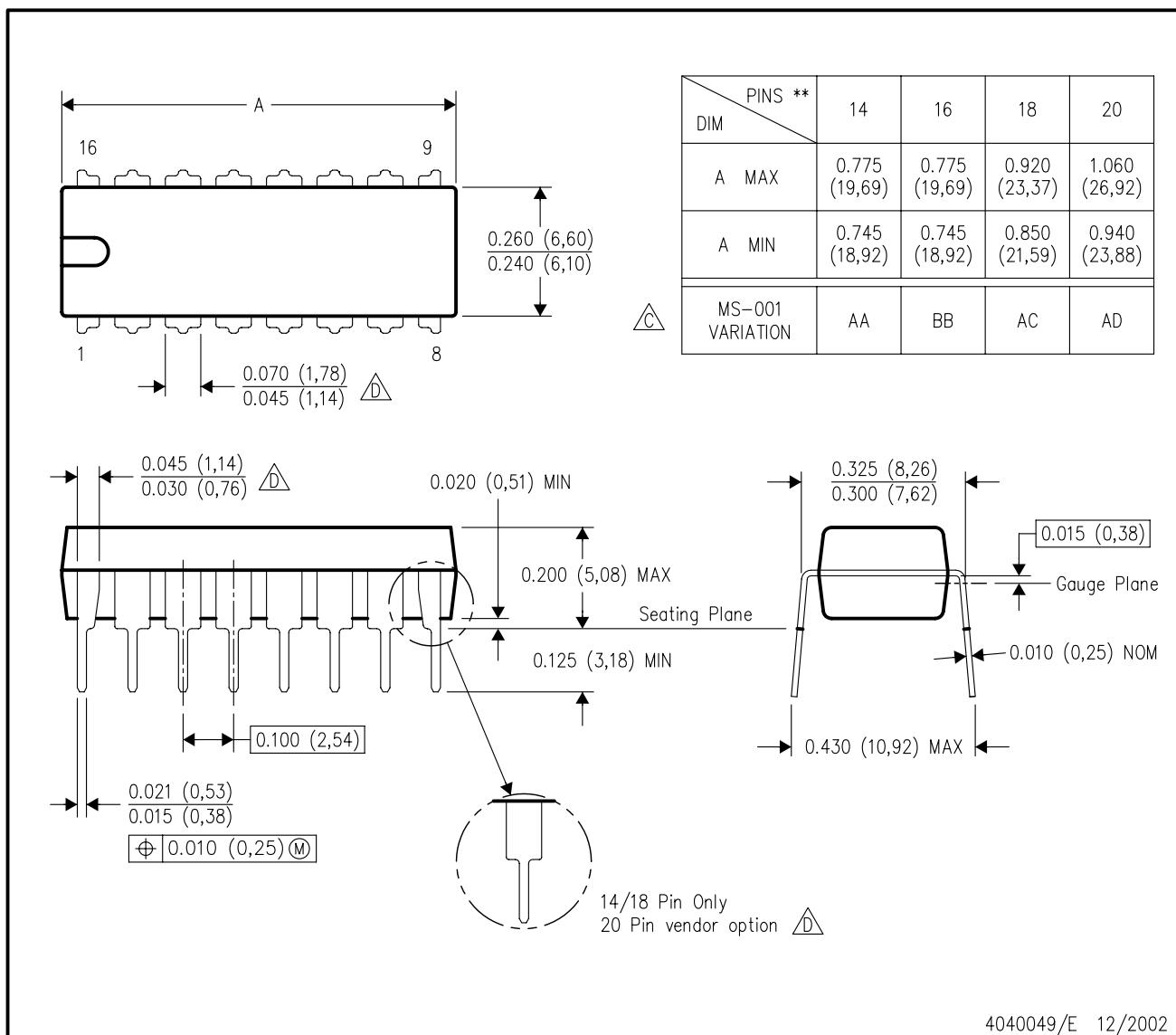
PACKAGE OPTION ADDENDUM

11-Apr-2013

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



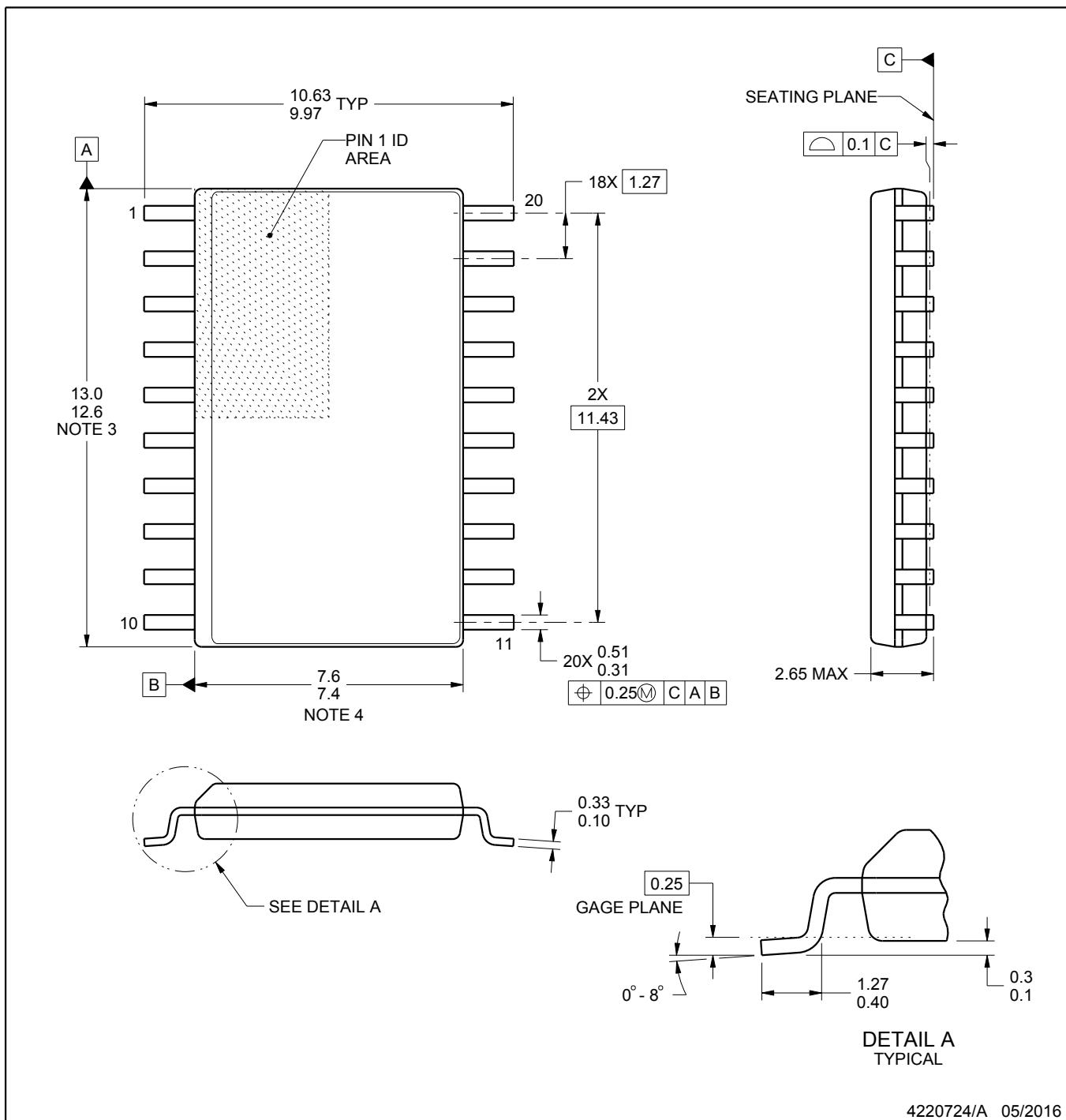
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

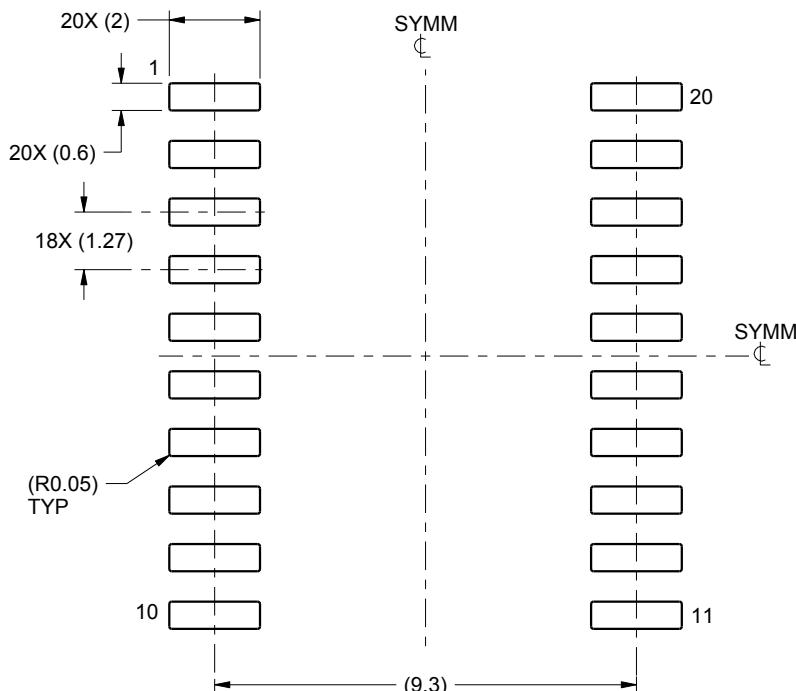
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

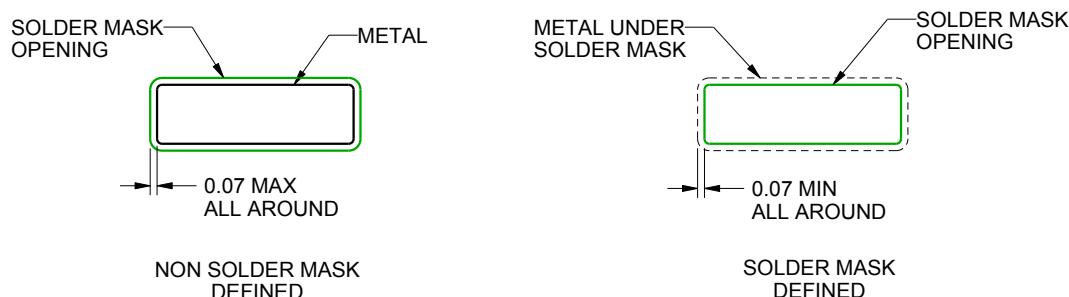
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

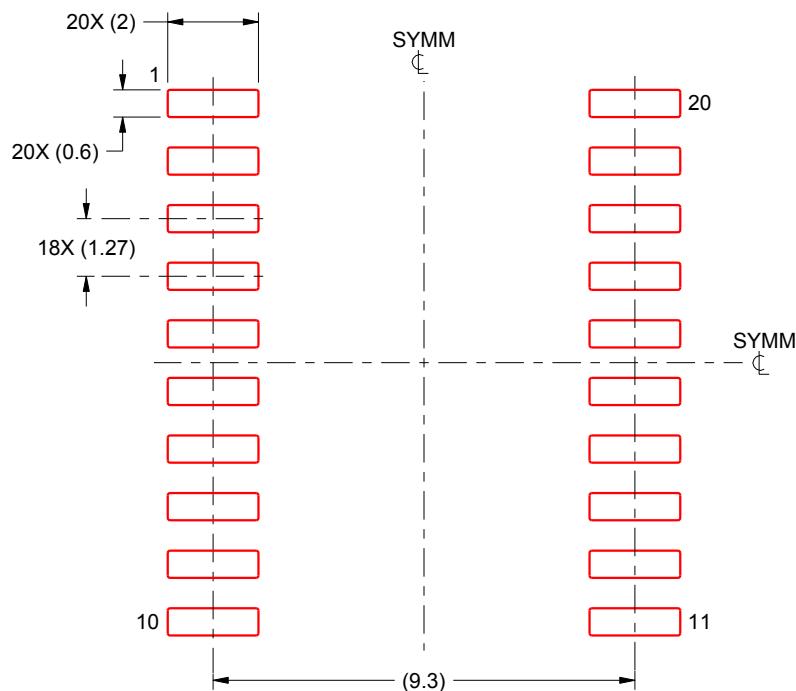
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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