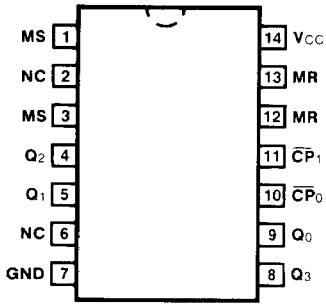
54/74290 01003
54LS/74LS290 01003

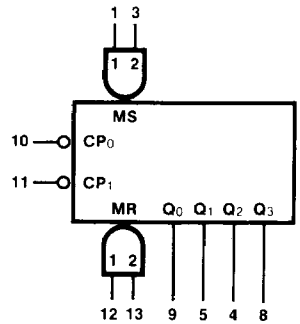
BCD DECADE COUNTER

DESCRIPTION — The '290 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-five. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state. HIGH signals on the Master Set (MS) inputs override the clocks and MR and force the outputs to the BCD nine state. The '290 is the same circuit as the '90 except that it has corner power pins and is therefore recommended for new designs. For detail specifications, truth tables and functional description, please refer to the '90 data sheet.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7
NC = Pin 2,6

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74290PC, 74LS290PC		9A
Ceramic DIP (D)	A	74290DC, 74LS290DC	54290DM, 54LS290DM	6A
Flatpak (F)	A	74290FC, 74LS290FC	54290FM, 54LS290FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.5
$\overline{CP}_1$	÷5 Section Clock Input (Active Falling Edge)	3.0/3.0	2.0/2.0
MR_1, MR_2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
MS_1, MS_2	Asynchronous Master Set (Set to 9) Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Flip-flop Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷5 Flip-flop Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.