

74F350

4-Bit Shifter with 3-STATE Outputs

General Description

The 74F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0 , S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-STATE outputs of different packages and using the Output Enable (OE) inputs as a third Select level. With appropriate interconnections, the 74F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

Features

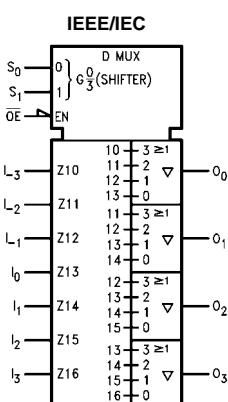
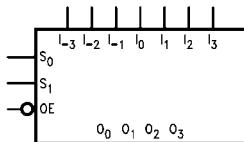
- Linking inputs for word expansion
- 3-STATE outputs for extending shift range

Ordering Code:

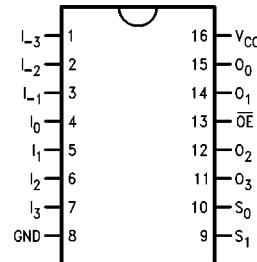
Order Number	Package Number	Package Description
74F350SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F350SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F350PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Truth Table

OE	S ₁	S ₀	Outputs			
			O ₀	O ₁	O ₂	O ₃
H	X	X	Z	Z	Z	Z
L	L	L	I ₀	I ₁	I ₂	I ₃
L	L	H	I ₋₁	I ₀	I ₁	I ₂
L	H	L	I ₋₂	I ₋₁	I ₀	I ₁
L	H	H	I ₋₃	I ₋₂	I ₋₁	I ₀

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S_0, S_1	Select Inputs	1.0/2.0	$20 \mu A/1.2 mA$
$I_{-3}-I_3$	Data Inputs	1.0/2.0	$20 \mu A/1.2 mA$
\overline{OE}	Output Enable Input (Active LOW)	1.0/2.0	$20 \mu A/1.2 mA$
O_0-O_3	3-STATE Outputs	150/40 (33.3)	$-3 mA/24 mA (20 mA)$

Functional Description

The 74F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 4-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1 . Outputs O_0-O_3 are 3-STATE, controlled by an active LOW output enable (\overline{OE}). When \overline{OE} is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be

logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

Logic Equations

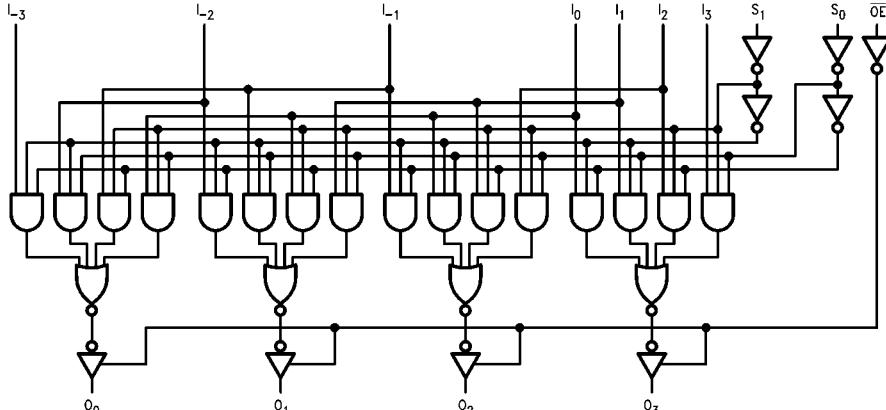
$$O_0 = \overline{S}_0 \overline{S}_1 I_0 + S_0 \overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$

$$O_1 = \overline{S}_0 \overline{S}_1 I_1 + S_0 \overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$

$$O_2 = \overline{S}_0 \overline{S}_1 I_2 + S_0 \overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$

$$O_3 = \overline{S}_0 \overline{S}_1 I_3 + S_0 \overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

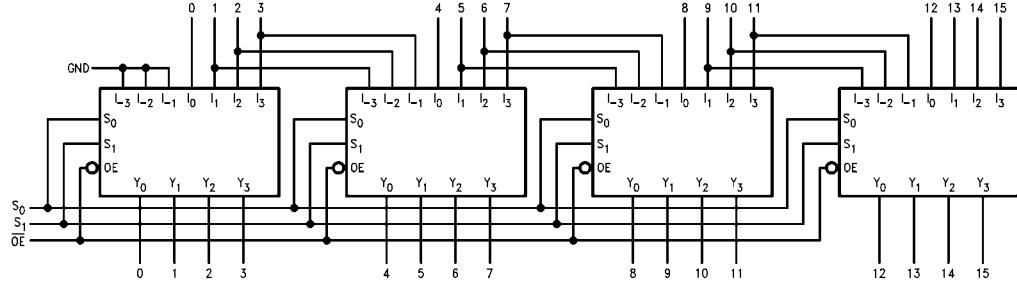
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Applications

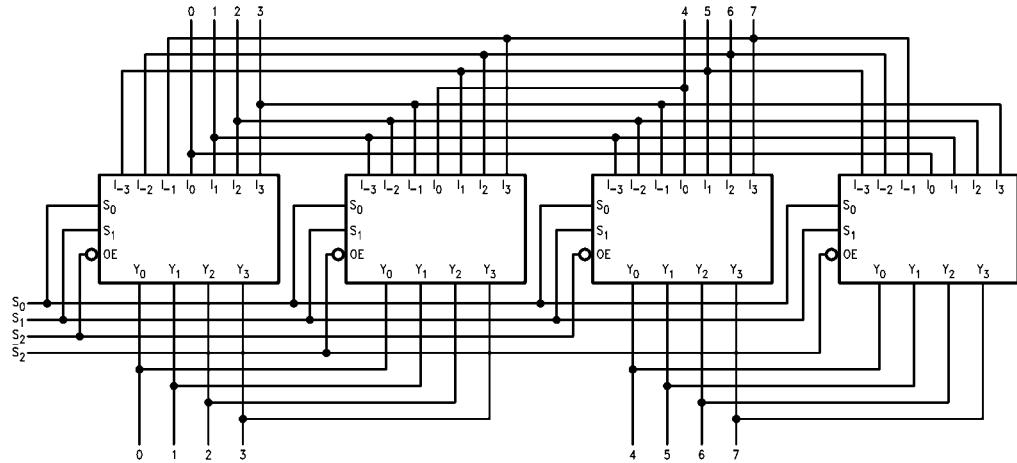
16-Bit Shift-Up 0 to 3 Places, Zero Backfill



Function Table

S_1	S_0	Shift Function
L	L	No Shift
L	H	Shift 1 Place
H	L	Shift 2 Places
H	H	Shift 3 Places

8-Bit End Around Shift 0 to 7 Places

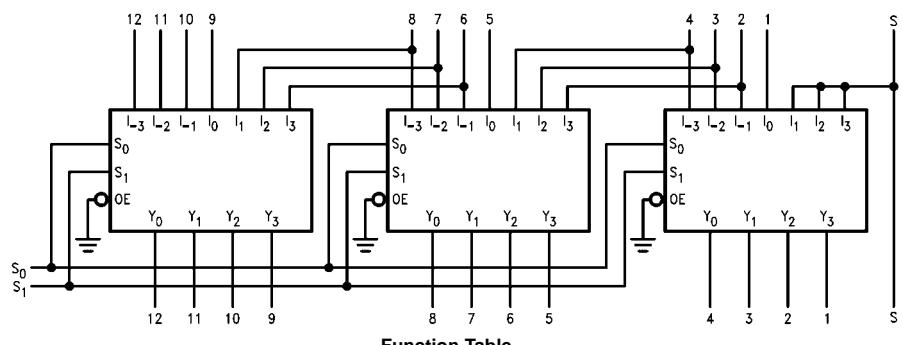


Function Table

S_2	S_1	S_0	Shift Function
L	L	L	No Shift
L	L	H	Shift End Around 1
L	H	L	Shift End Around 2
L	H	H	Shift End Around 3
H	L	L	Shift End Around 4
H	L	H	Shift End Around 5
H	H	L	Shift End Around 6
H	H	H	Shift End Around 7

74F350

13-Bit Twos Complement Scaler



Function Table

S ₁	S ₀	Scale
L	L	1/8
L	H	1/4
H	L	1/2
H	H	1

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	
Standard Output	-0.5V to V_{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

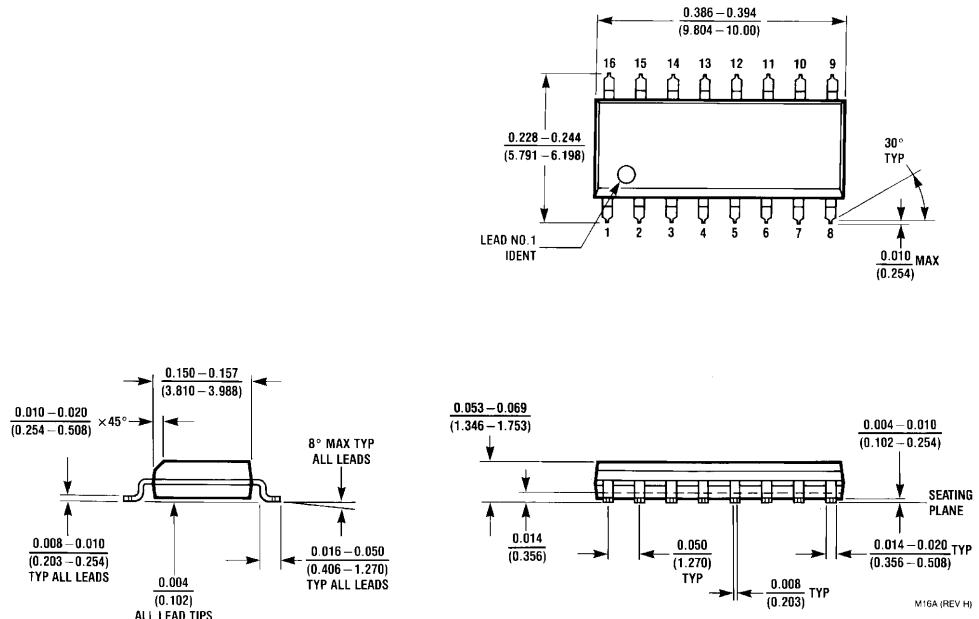
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

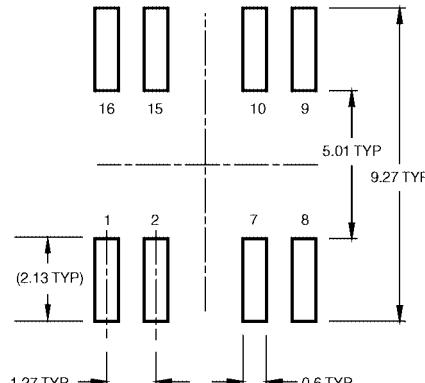
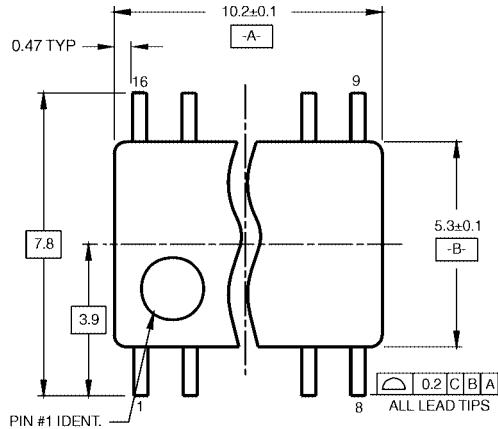
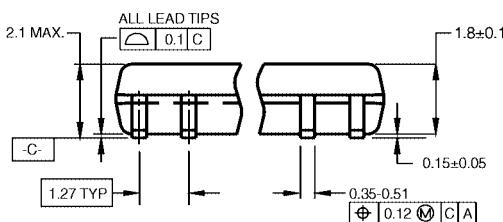
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5				$I_{OH} = -1$ mA
		10% V_{CC}	2.4				$I_{OH} = -3$ mA
		5% V_{CC}	2.7				$I_{OH} = -1$ mA
		10% V_{CC}	2.7				$I_{OH} = -3$ mA
V_{OL}	Output LOW Voltage	10% V_{CC}		0.5	V	Min	$I_{OL} = 24$ mA
I_{IH}	Input HIGH Current			5.0	μ A	Max	$V_{IN} = 2.7V$
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μ A	Max	$V_{IN} = 7.0V$
I_{CEX}	Output HIGH Leakage Current			50	μ A	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9$ μ A All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	μ A	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current			-1.2	mA	Max	$V_{IN} = 0.5V$
I_{OZH}	Output Leakage Current			50	μ A	Max	$V_{OUT} = 2.7V$
I_{OZL}	Output Leakage Current			-50	μ A	Max	$V_{OUT} = 0.5V$
I_{OS}	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0V$
I_{ZZ}	Bus Drainage Test			500	μ A	0.0V	$V_{OUT} = 5.25V$
I_{CCH}	Power Supply Current		34	42	mA	Max	$V_O = HIGH$
I_{CCL}	Power Supply Current		40	57	mA	Max	$V_O = LOW$
I_{CCZ}	Power Supply Current		40	57	mA	Max	$V_O = HIGH$ Z

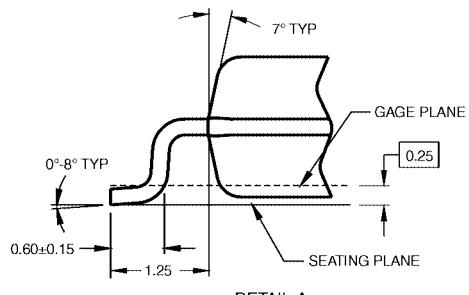
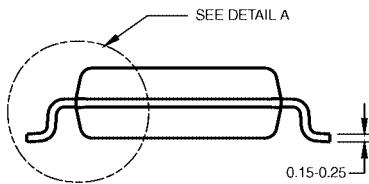
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			$T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay I_n to O_n	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.0 6.5	ns
t_{PLH}	Propagation Delay S_n to O_n	4.0 3.0	7.8 6.5	10.0 8.5	4.0 3.0	13.5 9.5	ns
t_{PZH}	Output Enable Time	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	8.0 10.0	ns
t_{PLZ}	Output Disable Time	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	6.5 7.5	

Physical Dimensions inches (millimeters) unless otherwise noted

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS



NOTES:

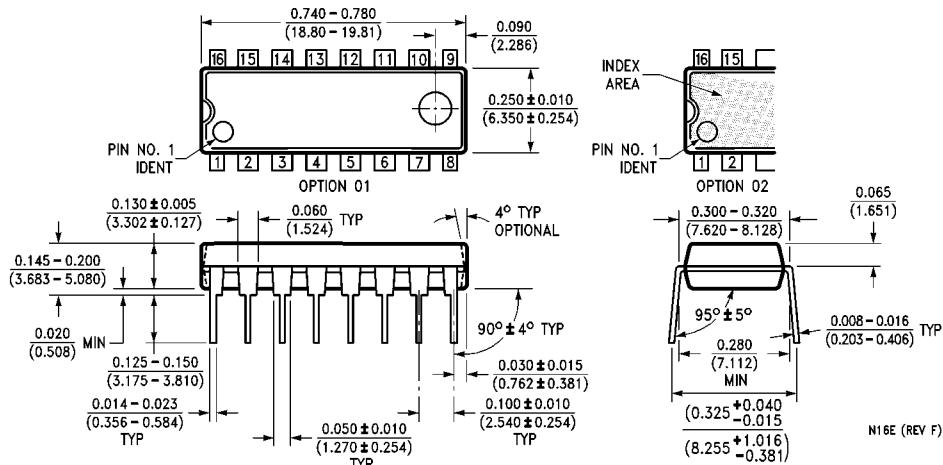
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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions

inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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