MOS DIGITAL INTEGRATED CIRCUIT
μPD1990AC

SERIAL I/O CALENDAR & CLOCK
CMOS LSI

The μPD1990AC is a CMOS integrated circuit having a clock function, which has been designed with the intent of connecting to microcomputer.

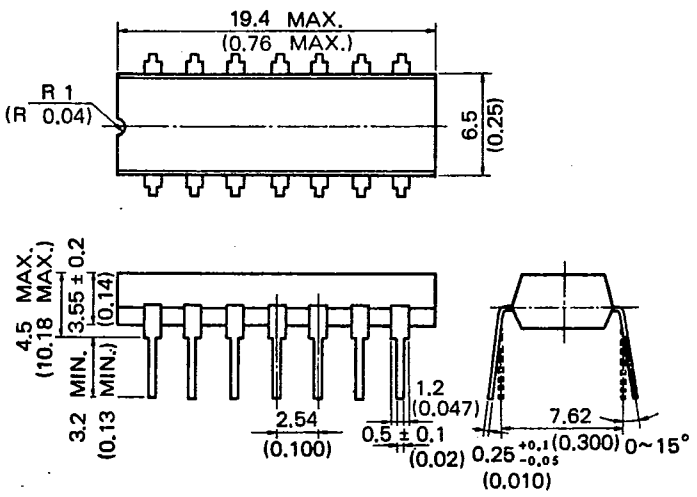
This IC counts independently the month, date, day of the week, hour, minute and second, and is able to have the output and input of these time data freely upon command from the microcomputer. By employing this IC, the microcomputer is freed from performing clock functions, and will be able to be use exclusively to other complicated operations.

The μPD1990AC employs the oscillation of a 32.768 kHz crystal as a reference. And all functions are enclosed in a 14 pin dual in-line package.

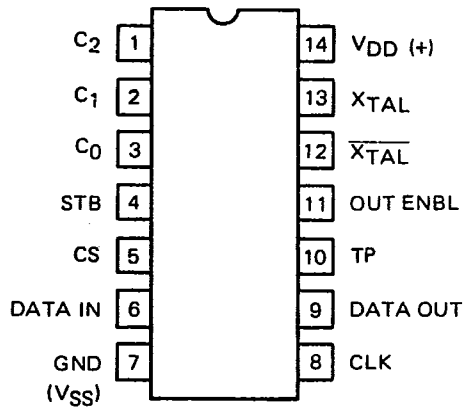
FEATURES

- Timekeeping (hours, minutes and seconds) and calendar (months, date and day of the week).
- Serial input and output of date.
  (Input & output code: All digits Binary Coded Decimal, except "Month" which is Hexa-Decimal Code)
- Reference frequency is 32.768 kHz, which is generated by a crystal oscillator circuit.
- Provided with timing pulse outputs. (Selection of 64 Hz, 256 Hz or 2 048 Hz is possible.)
- By using CS (chip selection) terminal, multi-chip applications are possible.

PACKAGE DIMENSIONS
in millimeters (inches)

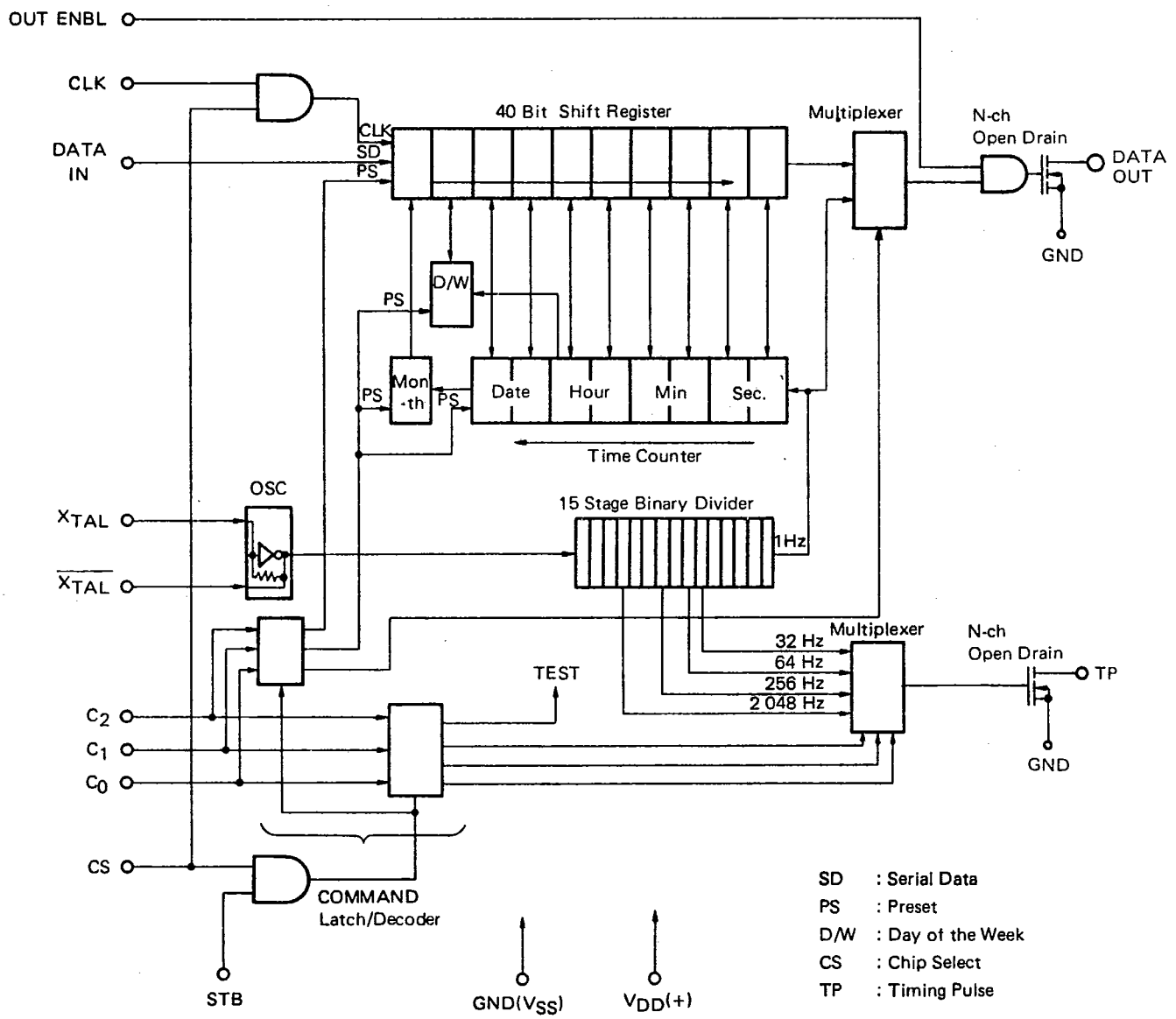


CONNECTION DIAGRAM (Top View)



NO.	Terminology	NO.	Terminology
1	C_2	8	CLK
2	C_1	9	DATA OUT
3	C_0	10	TP
4	STB	11	OUT ENBL
5	CS	12	$\overline{X_{TAL}}$
6	DATA IN	13	X_{TAL}
7	GND(V_{SS})	14	V_{DD} (+)

SERIAL I/O CALENDAR BLOCK DIAGRAM



f_{osc} = 32.768 kHz
V_{DD} = 2.0 to 5.5 V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$V_{DD}-V_{SS}$	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating Temperature Range	T_{opt}	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Output Terminal Voltage	V_{OUT}	$V_{SS}-0.3$ to 6.0	V

ELECTRICAL CHARACTERISTICS (f=32.768 kHz, $C_G=C_D$=20 pF, Xtal R_S=20 kΩ, Ta=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Operating Voltage	$V_{DD}-V_{SS}$	2.00		5.50	V	
Current Consumption	I_{SS}		20	50	μA	$V_{DD}-V_{SS}$=3.60 V
Low Level Output Current	I_{OL}	*500			μA	$V_{DD}-V_{SS}$=2.0 V V_{OL}=0.4 V
CLK Input Frequency	f_{CLK}	DC		100	kHz	$V_{DD}-V_{SS}$=2.0 V, Duty 50 %
Input Leakage Current	I_{IN}			1	μA	$V_{DD}-V_{SS}$=3.60 V
High Level Input Voltage	V_{IH}	$0.8V_{DD}$		V_{DD}	V	
Low Level Input Voltage	V_{IL}	V_{SS}		$0.2V_{DD}$	V	
Oscillation Starting Voltage	V_{STA}	2.0			V	T_{STA}=10 s

* TP and DATA OUT are N-channel open drain output.

A.C. ELECTRICAL CHARACTERISTICS (FOR REFERENCE --- NOT SPECIFIED)

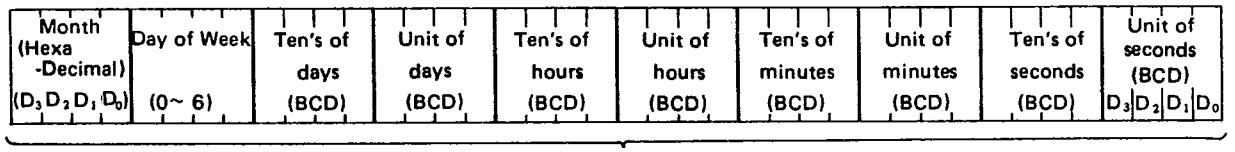
(f=32.768 kHz, $V_{DD}-V_{SS}$=2.0 V, Ta=25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_0~2, CS–STB Set-up Time	t_{SU}	2			μs	
STB Pulse Width	T_{STB}	2			μs	
C_0~2, CS–STB Hold Time	T_{HLD}	2			μs	
STB LATCH Delay Time	t_{d1}			*4	μs	except Time Read mode
CLK–DATA OUT Delay Time	t_{dc-o}			2	μs	R_L=33 kΩ, C_L=15 pF
DATA IN Set-up Time	t_{DSU}	2			μs	
DATA IN Hold Time	t_{DHLD}	2			μs	

* Note: When group 0 is Time Read mode, STB LATCH delay time is 40 μs MAX. (t_{d2}).

FUNCTION SPECIFICATIONS

- Reference frequency (X tal osc.).
  - 32.768 kHz
- Data.
  - Hours, Minutes, Seconds, Months, Date and Days of the Week ("Hours" 24 hour form) (Automatic adjustment of long and short months). The data is output in order to "Second", "Minute", "Hour", "Day", "Day of Week", "Month". Refer to Fig. 1.
- Data format
  - Binary Coded Decimal (except "Month" which is Hexa-Decimal Code)
- Data input-output and Clock.
  - Serial input, serial output.
  - Data input and output in synchronization with the clock input from the CLK.
- Timing pulse output.
  - One of 64 Hz, 256 Hz or 2 048 Hz can be selected by command.
- Mode selection.
  - Selected according to input to C_0, C_1, C_2.
    Group "0" C_2=0 Register control (control of data input-output).
    Group "1" C_2=1 Tp selection (Selection of timing pulses) and TEST MODE setting.
  - Commands of group "0" and those of group "1" are independently latched by the STB input.
- Chip select.
  - CLK and STB inputs prohibited by connecting CS input to GND(V_{SS}) level.
- Prohibition of output of data.
  - Making OUT ENBL input GND level DATA OUT terminal become high impedance.
- Leap year
  - The correction for length of the month is automatically performed and leap year is not automatically performed. But it is possible to set calendar FEB. 29, and the day after, it will be Mar. 1.



40 Bit Shift Register

* DATA of 40 Bit Shift Register appears on DATA OUT terminal from LSB of Second.

Fig. 1

TERMINALS

- Input terminals.
  - DATA IN — Data input of 40 bit shift register.
  - CLK — Shift clock input of 40 bit shift register.
  - $C_0 \sim C_2$ — Command input (3 bit).
  - STB — Strobe input.
  - CS — Chip select input (Prohibits CLK & STB).
  - OUT ENBL — Output control input (Makes the DATA OUT high impedance by inputting low level).
- Output terminals. (N-channel Open Drain)
  - DATA OUT — Data output of 40 bit shift register.
  - TP — Time pulse output.
- Oscillation terminals.
  - XTAL — Oscillation inverter input (OSC IN).
  - $\overline{XTAL}$ — Oscillation inverter output (OSC OUT).
- Power supply terminals.
  - V_{DD} — Plus power supply.
  - GND (V_{SS}) — Common line.

COMMAND SPECIFICATIONS

Group	C_2	C_1	C_0	FUNCTION	
0	0	0	0	Register Hold (TEST MODE is released)	DATA OUT = 1 Hz
	0	0	1	Register Shift	DATA OUT = [LSB]
	0	1	0	Time Set & Counter Hold	DATA OUT = [LSB]
	0	1	1	Time Read	DATA OUT = 0.5 Hz
1	1	0	0	TP = 64 Hz Set (TEST MODE is released)	
	1	0	1	TP = 256 Hz Set (TEST MODE is released)	
	1	1	0	TP = 2 048 Hz Set (TEST MODE is released)	
	1	1	1	TEST MODE Set	

* Groups "0" and "1" hold their functions independently, in other word, the command of the group "0" ("1") can change the group "0" ("1") function mode only. Then you must release the μPD1990AC from TEST MODE by setting commands of TP selection (group "1") or Register Hold Mode.

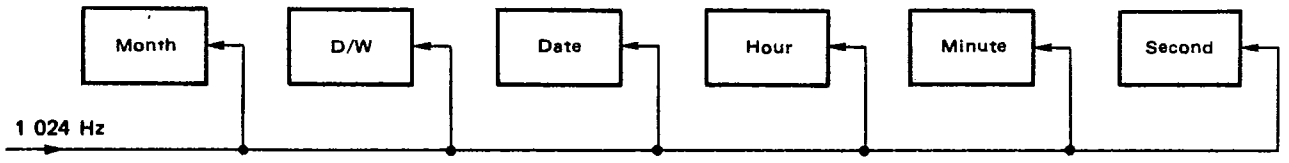
- Command input.
  - 3 bit, binary code input. C_0, C_1, C_2
- Number of commands.
  - Register control — 4
  - TP control — 3
  - TEST MODE set — 1

  } 8

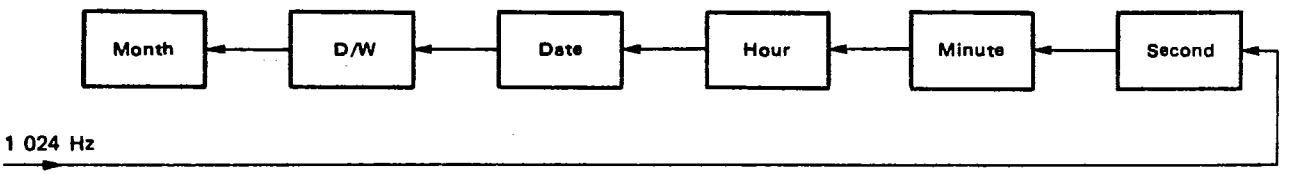
- Commands.
  - Register control [Group "0"]
    - ★ Register Hold MODE [0 0 0]
      Holds the 40 Bit Shift Register.
      The data is held, and shifting of the data becomes impossible.
      1 Hz is output from the DATA OUT terminal. The TEST MODE is released by this command.
    - ★ Shift MODE [0 0 1]
      Shifting of data of the 40 Bit Shift Register becomes possible.
      Data is shifted in synchronization with the clock input on CLK terminal.
      DATA OUT terminal outputs data from [LSB] of the 40 Bit Shift Register.
    - ★ Time set MODE [0 1 0]
      Presets the data of the 40 Bit Shift Register in the Time Counter.
      Resets the Flip-Flop (F/F) of 11 to 15 bits of the 15 Stage Binary Divider and hold the Time Counter.
      By setting other command of group "0", the Time Counter is released from the reset and the hold.
      [LSB] is output from the DATA OUT terminal.
      Shifting of data becomes impossible.
    - ★ Time read MODE [0 1 1]
      Reads into the 40 Bit Shift Register the data of the Time Counter.
      DATA OUT terminal outputs the data of [LSB] ([LSB]=0.5 Hz). Shifting of data becomes impossible.
  - TP control [Group "1"]
    - ★ TP = 64 Hz set MODE [1 0 0]
      64 Hz (duty 50 %) is output from the TP terminal.
    - ★ TP = 256 Hz set MODE [1 0 1]
      256 Hz (duty 50 %) is output from the TP terminal.
    - ★ TP = 2048 Hz set MODE [1 1 0]
      2048 Hz (duty 50 %) is output from the TP terminal.
    - ★ TEST MODE set MODE [1 1 1]
      Sets up the TEST MODE (Not used for ordinary operation). When TEST MODE is released by Register Hold MODE [000], TP terminal is 64 Hz output.

- TEST MODE (Set by command of TEST mode (111))
  In this mode DATA OUT terminal is enabled in spite of OUT ENBL input.
  There are 2 type TEST MODE selected by OUT ENBL terminal.

  TEST MODE 1 ; OUT ENBL = 0
  In this mode every Counter ("Month", "Day of Week", "Date", "Hour", "Minute", "Second") is advanced at a 1 024 Hz in parallel. In this case overflow carry of each counter is not affect to the next counter.



  TEST MODE 2 ; OUT ENBL = 1
  In this mode TIME COUNTER is advanced at 1 024 Hz in stead of 1 Hz from "Second" counter input.



Following table shows the signals appeared on DATA OUT and TP terminals during the μPD1990AC is in the TEST MODE.

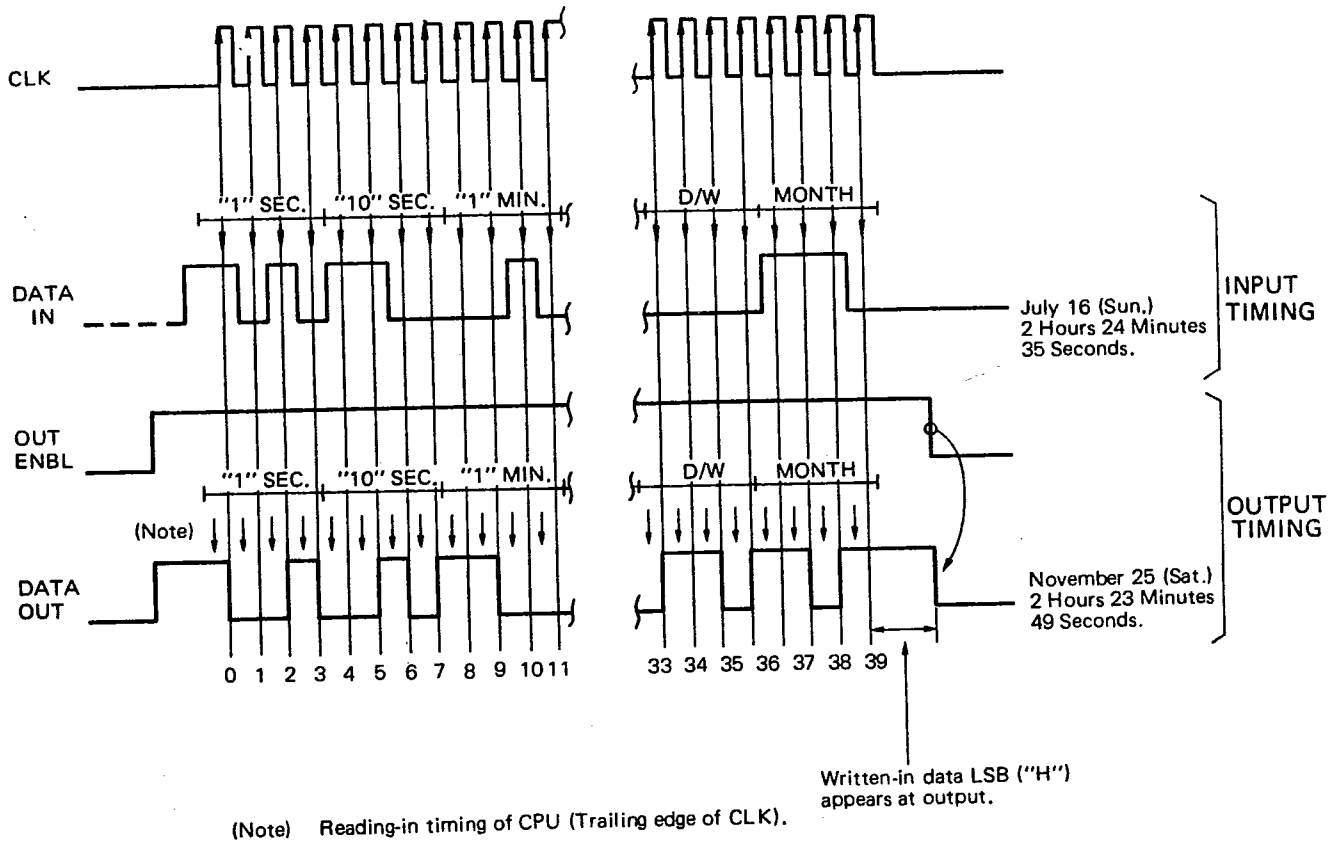
MODE	CODE C_2 C_1 C_0	DATA OUT	TP	OTHERS	
REGISTER HOLD	0 0 0	1 Hz	64 Hz	*By this command, TEST MODE is released.	
REGISTER SHIFT	0 0 1	LSB of 40 Bit S/R "0" or "1"	32 Hz	TEST MODE is remained.	T/C is advanced at 1 024 Hz in parallel or serial.
TIME SET	0 1 0	LSB of 40 Bit S/R "0" or "1"	32 Hz		
TIME READ	0 1 1	512 Hz	32 Hz		T/C is advanced at 1 024 Hz in parallel or serial.

S/R = Shift Register
T/C = Time Counter

*Note: While μPD1990AC is TEST Mode, by setting the Register Hold mode (Group "0" mode), Test Mode changes TP=64 Hz mode in group "1" and as a result Register Hold mode is set. 1 Hz appears on DATA OUT terminal and 64 Hz appears on TP terminal.

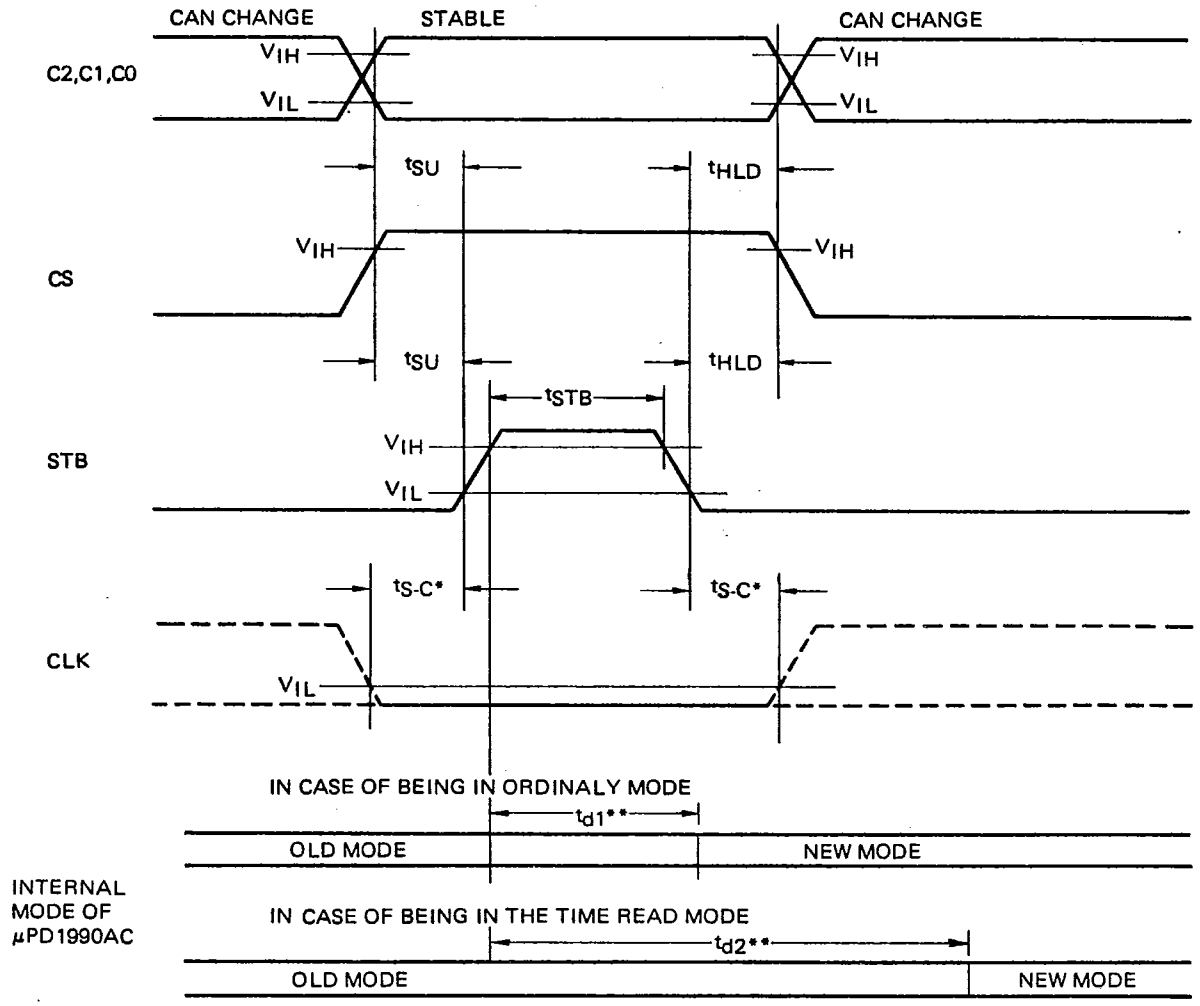
DATA INPUT/OUTPUT TIMING DIAGRAM

Command (C_2, C_1, C_0) is set to [001] (Shift Mode).
CS = "H"



(Note) Reading-in timing of CPU (Trailing edge of CLK).

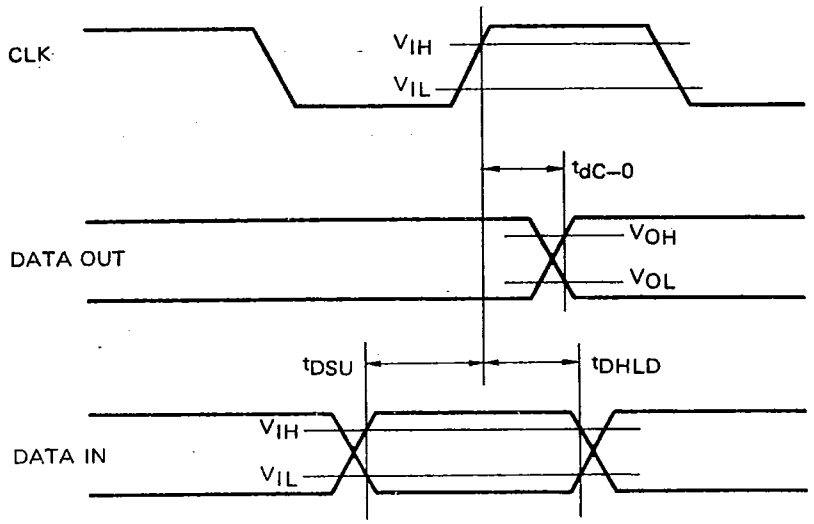
TIMING DIAGRAM FOR SETTING COMMANDS



t_{SU} = 2 μs MIN.
t_{HLD} = 2 μs MIN.
t_{STB} = 2 μs MIN.
t_{d1} = 4 μs MAX. (In case of being in ordinaly mode.)
t_{d2} = 40 μs MAX. (In case of being in the Time Read mode.)
t_{S-C} = 2 μs MIN.

Note: * Setting Register Shift command (001), input level of the CLK must be low level.
** The delay time until new mode becomes valid is 4 μs. MAX. (t_{d1}). But in the case of μPD1990AC being in the Time Read mode, it takes 40 μs MAX. (t_{d2}).

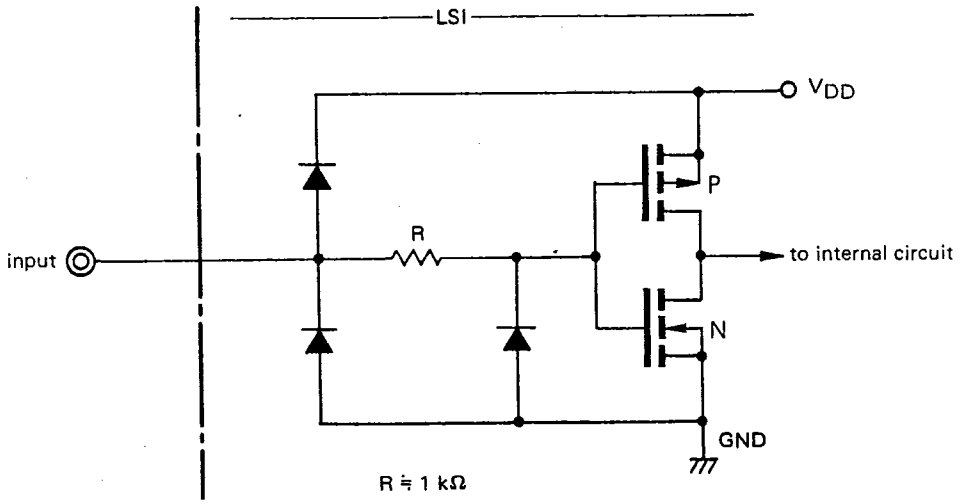
TIMING DIAGRAM OF DATA INPUT AND OUTPUT



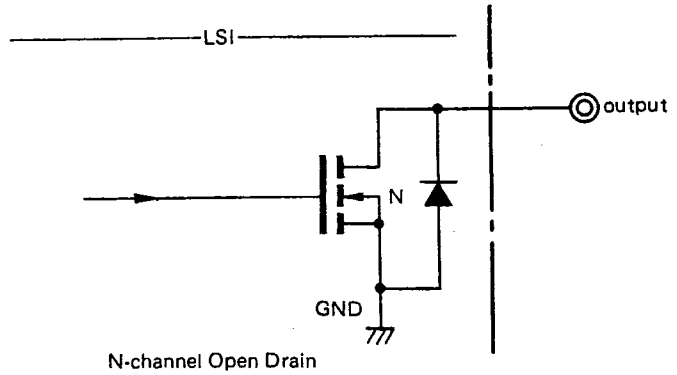
t_{dC-0} : 2 μs MAX. (RL=33 kΩ, CL=15 pF)
t_{DSU} : 2 μs MIN.
t_{DHLD} : 2 μs MIN.

INPUT AND OUTPUT CIRCUITS FOR μPD1990AC

Input circuits
(for C2, C1, C0, STB, DATA IN, CLK, OUT ENBL, CS)

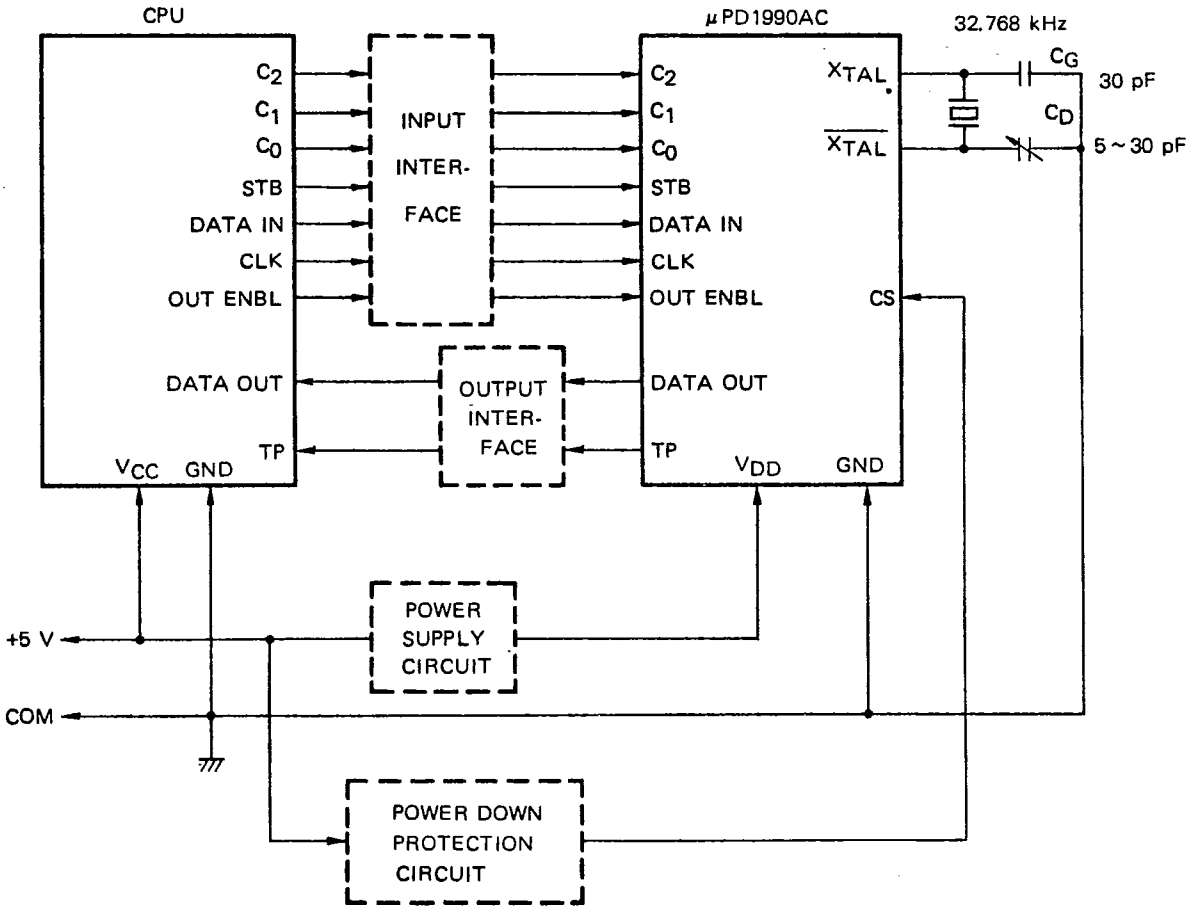


Output circuits
(for DATA OUT, TP terminals)

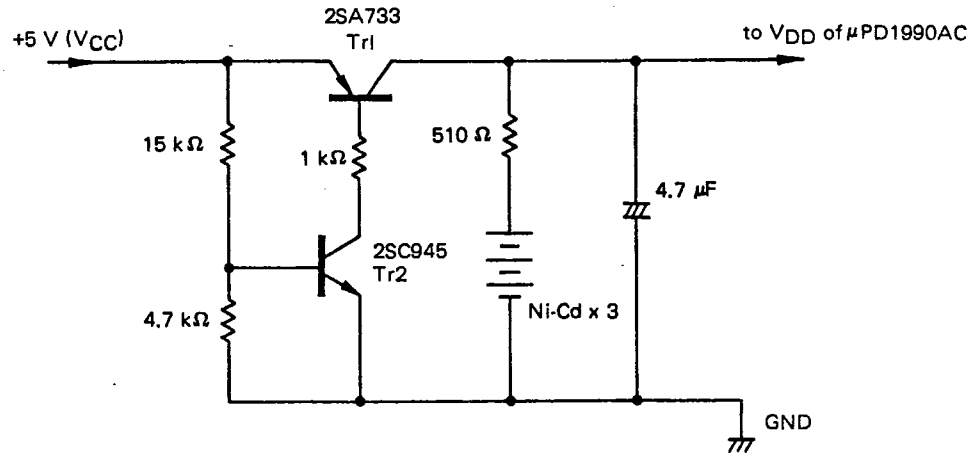


N-channel Open Drain

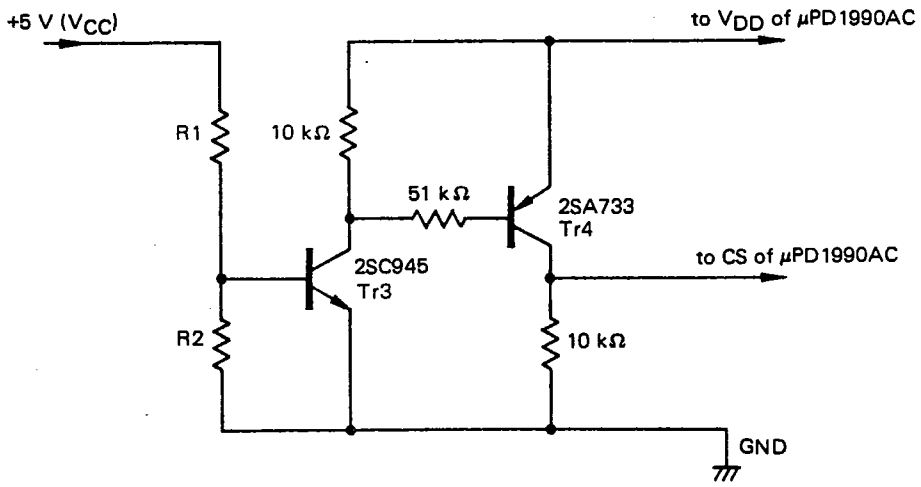
APPLICATION CIRCUIT



POWER SUPPLY CIRCUIT



POWER DOWN PROTECTION CIRCUIT

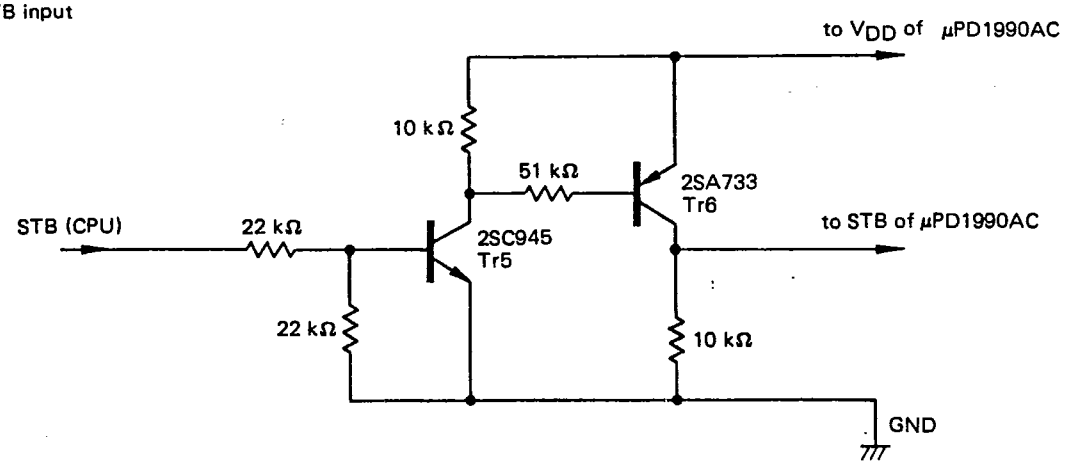


The Power Down of V_{CC} line makes CS terminal inactive, with R1 and R2 resistors. The trigger level of this circuit is calculated as following.

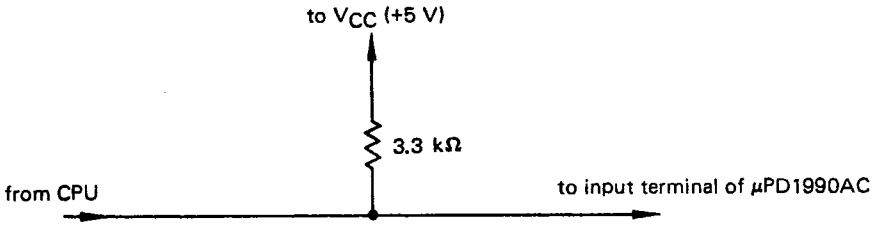
$$V_{trigger} = \frac{(R1+R2)\cdot V_{BE}Tr3}{R2}$$

INPUT INTERFACE

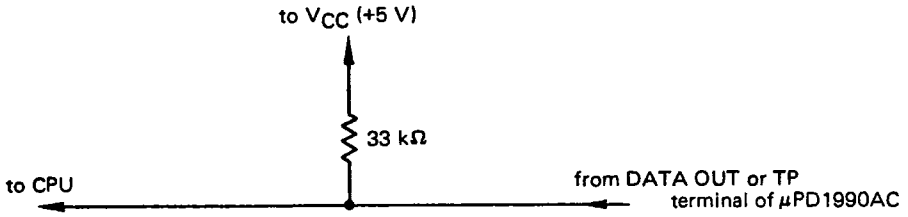
For STB input



For other input (C2, C1, C0, DATA IN, CLK, OUT ENBL)



OUTPUT INTERFACE (DATA OUT, TP)



APPLICATION