CSS555C Micropower Timer (with Internal Timing Capacitor)

GENERAL PART DESCRIPTION

The CSS555C is a micropower version of the popular 555 timer IC. It features an operating current under 5µA and a minimum supply voltage of 1.2V, making it ideal for battery-operated applications. A six-decade programmable counter is included to allow generation of long timing delays. Configuration data for the counter is held in EEPROM to maintain the standard pin count of eight. The analog circuits are temperature compensated to provide excellent stability over a wide ambient temperature range. A simple four-wire interface provides Read/Write access to the EEPROM. The CSS555C device includes an internal precision timing capacitor (C_{TI}). Its value is trimmed to 100pF ±1%.

Key Features

- Lowest power 555 timer (by > 10X)!
  Active mode current < 5 µA
- Wide operating range
  Wide supply range: 1.2V to 5.5V
  Temperature range: -40℃ to +85℃
- Internal 6 decade, programmable counter
  Settings = 1, 10, 10^2, 10^3, 10^4, 10^5 & 10^6
  Multiplies delay time by up to 10^6
  Delay times from microseconds to days
- Internal 100pF, ±1% Timing Capacitor
  User adjustable, 0.2pF resolution
- Pin-for-pin compatible with 555 series timers
  Monostable or Astable operation
- Extremely low transient switching current
  "Break-Before-Make" output driver
- Temperature stability – 0.005% per ℃

Applications

- Portable & Battery-Powered Systems
- Precision Timing & Pulse Generation
- Ultra Long Period Delay Generation
- Single Cell Battery Applications
- Ultra Low Power Timers
- Pulse Width Modulation
- Low Cost, High Reliability Applications

Pin Configuration

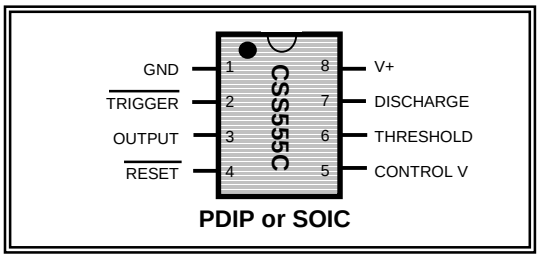


Figure 1

Typical Application Circuit

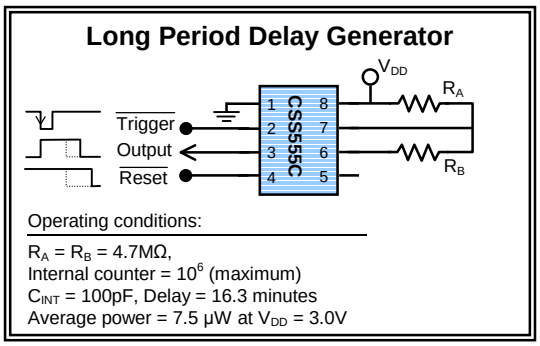


Figure 2

Ordering Information

Part Number	Package Description
CSS555C-ID	8 pin plastic DIP
CSS555C-IS	8 pin plastic SOIC

See page 9 for more details and options.

Custom Silicon Solutions Inc.
17951 Sky Park Circle, Suite F
Irvine, CA 92614
(949) 797-9220 • FAX: (949) 797-9225 • www.CustomSiliconSolutions.com

Block Diagrams

Standard 555 Timer Configuration (Std. Mode)

(Programmable counter bypassed, Divider setting = 1)

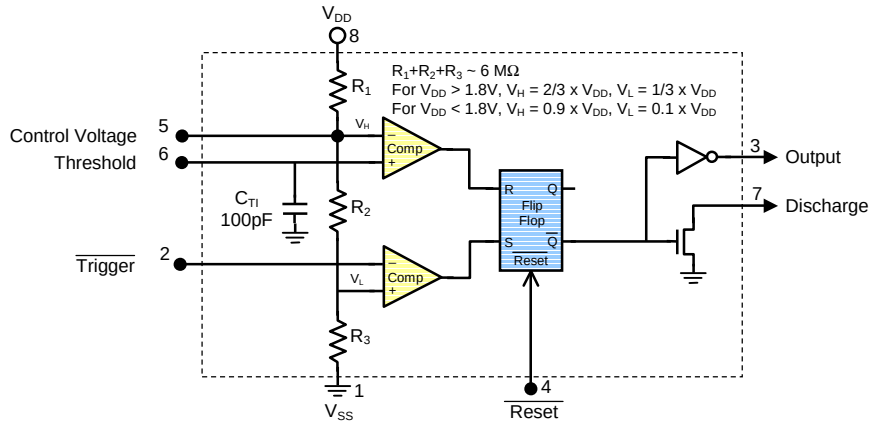


Figure 3

Extended Period Configuration (EP Mode)

(Programmable counter enabled, Divider setting ≥ 10)

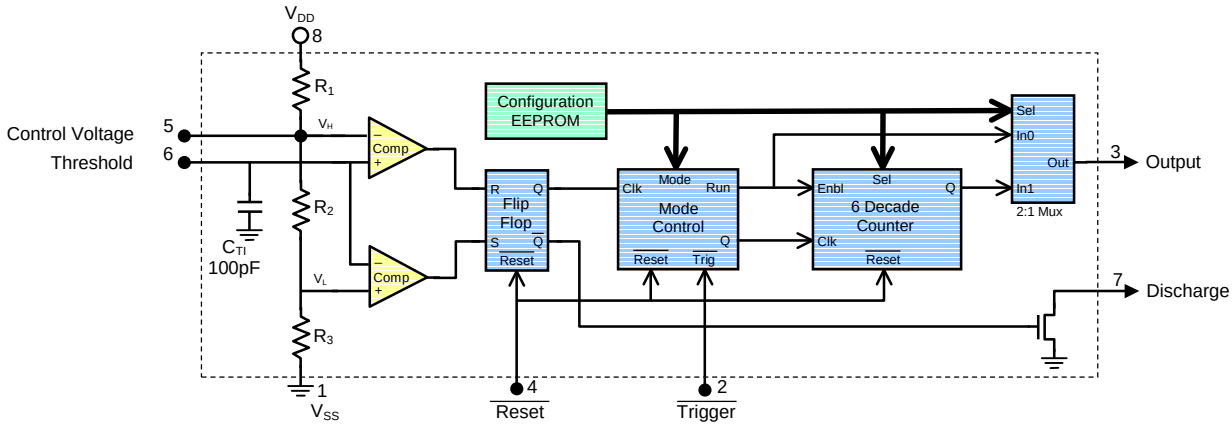


Figure 4

EEPROM Bit Assignments

Counter Configuration	Divider Setting (Mult)
xxxxx000	1 (Std. 555)
xxxxx001	10
xxxxx010	100
xxxxx011	1K
xxxxx100	10K
xxxxx101	100K
xxxxx110	1M
xxxxx111	1 (Std. 555)

Table 1A

Mode Control Bits	Function
xxxx0xxx	Astable Mode (“Don’t Care” if Std. 555)
xxxx1xxx	Monostable Mode (“Don’t Care” if Std. 555)
xxx0xxxx	Micro Power
xxx1xxxx	Low Power
xx0xxxxx	Standard Voltage (Trip levels = ⅓ & ⅔ V_{DD})
xx1xxxxx	Low Voltage (Trip levels = 10% & 90% V_{DD})
Bit 6	Unused
Bit 7	1 (Read Only)

Table 1B

Note: For detailed programming information, see Application Note AN555-1 (CSS555_App_Note1_Serial_Interface)

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Supply Voltage (V_{DD})	6V
Voltage at any Pin	-0.3 to V_{DD} +0.3V
Total Current into V_{DD} Pin (Source)	50 mA
Total Current out of GND Pin (Sink)	60 mA
Storage Temperature Range	-65℃ to +140℃

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

Electrical Characteristics

Temperature = 25℃, Test Circuit #1, unless otherwi se specified
(If VDD < 1.8V, "Low Voltage" mode must be selected to provide adequate comparator input levels. EE Bit5 = 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Range	VDD	Standard VDD (EE Bit 5 = 0)	1.8		5.5	V
		Low VDD (EE Bit 5 = 1)	1.2		5.5	V
Supply Current	IDD	V_{DD} = 1.5V		2.2	4.0	µA
(No DC load on OUTPUT pin, $R_L = \infty$)		V_{DD} = 3.0V		3.1	6.0	µA
		V_{DD} = 5.0V		4.3	8.0	µA
Timing Accuracy	TA_{VDD}	$R_{A(B)}$ = 1MΩ, C_T = 0.001µF				
(Micro power setting, EE Bit 4 = 0)		V_{DD} = 1.5V		1.0	2.0	%
(Monostable & Astable Modes)		V_{DD} = 3.0V		1.0	2.0	%
		V_{DD} = 5.0V		1.0	2.0	%
Timing Drift with Temperature	TD_{TEMP}	$R_{A(B)}$ = 1MΩ, C_T = 0.001µF				
(Monostable & Astable Modes)		V_{DD} = 1.5V		45		ppm/℃
		V_{DD} = 3.0V		35		ppm/℃
		V_{DD} = 5.0V		35		ppm/℃
Timing Shift with Supply Voltage	TS_{VDD}	$R_{A(B)}$ = 1MΩ, C_T = 0.001µF				
(Monostable & Astable Modes)		V_{DD} = 1.5V		0.10		%/V
		V_{DD} = 3.0V		0.15		%/V
		V_{DD} = 5.0V		0.15		%/V
Maximum Oscillator Frequency	f_{MAX}	$R_{A,B}$ = 4.7KΩ, C_{TI} = 100 pF		1		MHz
Control Voltage	V_{CTRL}	Standard VDD (EE Bit 5 = 0)	64	67	70	% V
		Low VDD (EE Bit 5 = 1)	88	90	92	% V
Trigger Voltage	V_{TRIG}	Standard VDD (EE Bit 5 = 0)	30	33	36	% V
		Low VDD (EE Bit 5 = 1)	8	10	12	% V
Reset Voltage	V_{RST}		0.3 x V_{DD}	0.5 x V_{DD}	0.7 x V_{DD}	V
Output Voltage	V_{OL}	V_{DD} = 1.5V, I_{SINK} = 1 mA		0.07	0.15	V
(Timer Output Pin)		V_{DD} = 3.0V, I_{SINK} = 4 mA		0.16	0.25	V
		V_{DD} = 5.0V, I_{SINK} = 10 mA		0.31	0.50	V
	V_{OH}	V_{DD} = 1.5V, I_{SOURCE} = 1 mA	1.35	1.40		V
		V_{DD} = 3.0V, I_{SOURCE} = 4 mA	2.75	2.85		V
		V_{DD} = 5.0V, I_{SOURCE} = 10 mA	4.50	4.73		V
Discharge Saturation Voltage	V_{DIS}	V_{DD} = 1.5V, I_{SINK} = 2.5 mA		0.07	0.15	V
(Discharge Output Pin)		V_{DD} = 3.0V, I_{SINK} = 10 mA		0.18	0.25	V
		V_{DD} = 5.0V, I_{SINK} = 25 mA		0.36	0.50	V
Input Current	I_{IN}	V_{DD} = 5.5V		10		pA
(Trigger, Reset & Threshold Inputs)		V_{IN} = 0.0V to 5.5V				
Discharge Leakage Current	I_{DIS}	V_{DD} = 5.5V		1	100	nA
Output Rise & Fall Times	t_R, t_F	V_{DD} = 3.0V, C_L = 10 pF		5		ns
Input Capacitance	C_{IN}			10		pF
Internal Timing Capacitor (NPO)	C_{TI}	Trim Resolution = 0.2pF	99	100	101	pF

Table 2

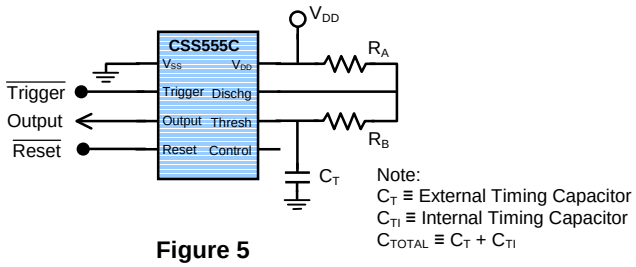
Electrical Characteristics (cont)

Temperature = -40℃ to +85℃, Test Circuit #1, unle ss otherwise specified
(If VDD < 1.8V, "Low Voltage" mode must be selected to provide adequate comparator input levels. EE Bit5 = 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Range	VDD	Standard VDD (EE Bit 5 = 0)	1.8		5.5	V
		Low VDD (EE Bit 5 = 1)	1.2		5.5	V
Supply Current	IDD	V_{DD} = 1.5V		2.2	5.0	µA
(No DC load on OUTPUT pin, $R_L = \infty$)		V_{DD} = 3.0V		3.1	7.5	µA
		V_{DD} = 5.0V		4.3	10.0	µA
Timing Accuracy	TA_{VDD}	$R_{A(B)}$ = 1MΩ, C_T = 0.001µF				
(Micro power setting, EE Bit 4 = 0)		V_{DD} = 1.5V		1.0	2.5	%
(Monostable & Astable Modes)		V_{DD} = 3.0V		1.0	2.5	%
		V_{DD} = 5.0V		1.0	2.5	%
Timing Drift with Temperature	TD_{TEMP}	$R_{A(B)}$ = 1MΩ, C_T = 0.001µF				
(Monostable & Astable Modes)		V_{DD} = 1.5V		45		ppm/℃
		V_{DD} = 3.0V		35		ppm/℃
		V_{DD} = 5.0V		35		ppm/℃
Timing Shift with Supply Voltage	TS_{VDD}	$R_{A(B)}$ = 1MΩ, C_T = 0.001µF				
(Monostable & Astable Modes)		V_{DD} = 1.5V		0.10		%/V
		V_{DD} = 3.0V		0.15		%/V
		V_{DD} = 5.0V		0.15		%/V
Maximum Oscillator Frequency	f_{MAX}	$R_{A,B}$ = 4.7KΩ, C_{TI} = 100 pF		1		MHz
Control Voltage	V_{CTRL}	Standard VDD (EE Bit 5 = 0)	64	67	70	% V
		Low VDD (EE Bit 5 = 1)	88	90	92	% V
Trigger Voltage	V_{TRIG}	Standard VDD (EE Bit 5 = 0)	30	33	36	% V
		Low VDD (EE Bit 5 = 1)	8	10	12	% V
Reset Voltage	V_{RST}		0.3 x V_{DD}	0.5 x V_{DD}	0.7 x V_{DD}	V
Output Voltage	V_{OL}	V_{DD} = 1.5V, I_{SINK} = 1 mA		0.07	0.20	V
(Timer Output Pin)		V_{DD} = 3.0V, I_{SINK} = 4 mA		0.16	0.30	V
		V_{DD} = 5.0V, I_{SINK} = 10 mA		0.31	0.60	V
	V_{OH}	V_{DD} = 1.5V, I_{SOURCE} = 1 mA	1.30	1.40		V
		V_{DD} = 3.0V, I_{SOURCE} = 4 mA	2.70	2.85		V
		V_{DD} = 5.0V, I_{SOURCE} = 10 mA	4.40	4.73		V
Discharge Saturation Voltage	V_{DIS}	V_{DD} = 1.5V, I_{SINK} = 2.5 mA		0.07	0.20	V
(Discharge Output Pin)		V_{DD} = 3.0V, I_{SINK} = 10 mA		0.18	0.30	V
		V_{DD} = 5.0V, I_{SINK} = 25 mA		0.36	0.60	V
Input Current	I_{IN}	V_{DD} = 5.5V		10		pA
(Trigger, Reset & Threshold Inputs)		V_{IN} = 0.0V to 5.5V				
Discharge Leakage Current	I_{DIS}	V_{DD} = 5.5V		1	100	nA
Output Rise & Fall Times	t_R, t_F	V_{DD} = 3.0V, C_L = 10 pF		5		ns
Input Capacitance	C_{IN}			10		pF
Internal Timing Capacitor (NP0)	C_{TI}	Trim Resolution = 0.2pF	99	100	101	pF

Table 3

Test Circuit #1



Note:
C_T ≡ External Timing Capacitor
C_{TI} ≡ Internal Timing Capacitor
C_{TOTAL} ≡ C_T + C_{TI}

Figure 5

Pin Descriptions

Pin Number	Pin Name	Primary Function (Normal Mode)	Secondary Function (EE Programming)
1	V_{SS}	Ground	
2	TRIGGER	Initiates timing cycles (Active low)	Serial Clock
3	OUTPUT	Timer Output (CMOS Levels)	Serial Data Out
4	RESET	Asynchronous timer reset (Active low)	Serial Data In
5	CONTROL V	Upper comparator switch level	R/W enable (Active if V_{CTRL} < 0.5V)
6	THRESHOLD	Upper comparator analog input	
7	DISCHARGE	Open drain FET, on when OUTPUT = 1	
8	V_{DD}	Positive voltage supply	

Table 4

Applications Information

General

The CSS555C IC may be used in many applications as a direct replacement for the popular 555 timer. It features the lowest 555 operating current and a minimum supply voltage of 1.2V. It also features a programmable decade counter for generating long time delays. An internal EEPROM stores the counter configuration: Divide by 1 (standard 555) or divide by 10, 100, 10^3, 10^4, 10^5 or 10^6. The internal counter allows long time delays to be generated with small value capacitors.

Monostable Operation

(Standard 555 Mode)

The circuit in Figure 6 shows a monostable or "one shot" configuration. A single, positive output pulse is generated on the falling edge of the TRIGGER input. When TRIGGER goes low, a flip-flop is set, the OUTPUT pin is set high and DISCHARGE allows the timing capacitor to charge towards V_{DD} via R_A. When V_{TH} reaches the upper comparator trip level, the flip-flop is reset, OUTPUT is forced low and DISCHARGE pulls V_{TH} to GND. After V_{TH} has discharged, the circuit is ready for the next trigger pulse. Typical signal waveforms are shown in Figure 7. The RESET input must be held high (inactive) during the timing cycle. If RESET is brought low, the OUTPUT pin is immediately forced low and the cycle is terminated.

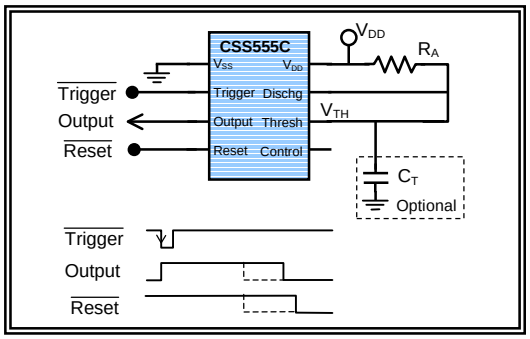


Figure 6 – Monostable Circuit (Std. Mode)

In the monostable configuration, the duration of the timing cycle is simply the time required to charge the timing capacitor from GND to the upper comparator trip level. The trip level is nominally ⅔ V_{DD}. At low supply voltages it is increased to 0.9 V_{DD}. (An EEPROM bit controls this selection.) The delay time equations for both conditions are provided in the following paragraph.

Delay Time Equations:

For standard supply voltages (V_{LOW} Bit = 0)

Charge time (V_{TH} = 0V to ⅔ V_{DD}) = 1.1 x R_A x C_{Total}

For low voltage mode (V_{LOW} Bit = 1)

Charge time (V_{TH} = 0V to 0.9 V_{DD}) = 2.3 x R_A x C_{Total}

where C_{Total} = ($C_{Internal}$ + $C_{External}$) or (C_{TI} + C_T)

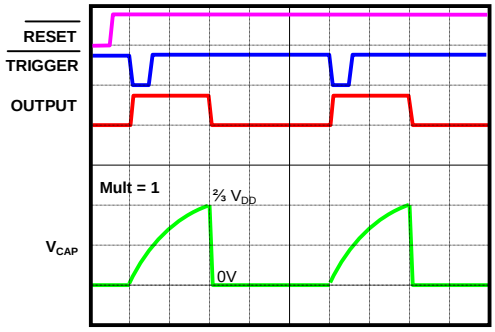


Figure 7 – Monostable Waveforms (Std. Mode)

Figure 8 provides a log-log selection chart. It shows the time delay for various combinations of R_A and C_{Total}. With the counter bypassed (Mult = 1), time delays from 1usec to 1 second are easily generated with capacitor values from 100pF to 1uF. For long time delays (or medium delay times using small capacitor values) the "Extended Period" configuration should be used. (See the next section.)

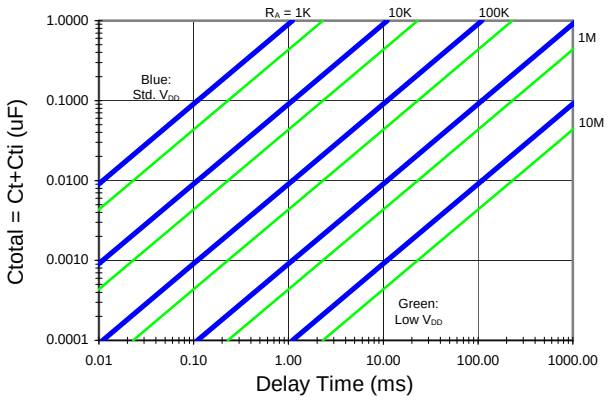


Figure 8 – Time Delay Chart

Monostable Operation

(Extended Period or "EP" Mode)

For longer time delays, the circuit in Figure 9 uses the internal decade counter to effectively multiply the value of the timing capacitor. Three bits in the EEPROM select a multiplier value from 10 to 10^6. The 555 analog block is configured as a free running oscillator, which is the input clock to the counter. On the falling edge of TRIGGER, the 555 oscillator is enabled, OUTPUT is set high, the decade counter is enabled and a new timing cycle begins. The timing cycle ends when the counter reaches the selected terminal count. Waveforms for an extended delay cycle are shown in Figure 10.

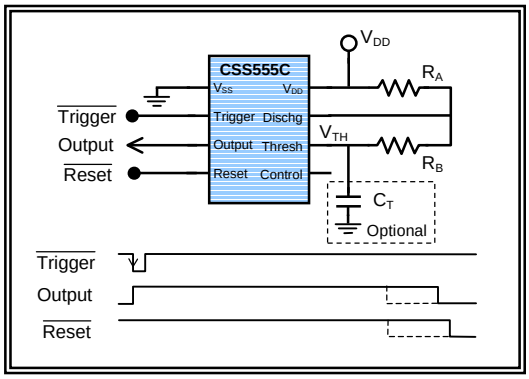


Figure 9 – Extended Period Delay Circuit

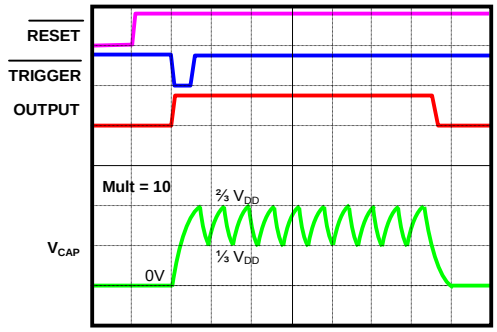


Figure 10 – Extended Period Waveforms

In the Extended Period monostable configuration, the duration of the timing cycle is the oscillator period multiplied by the counter setting. The 555 oscillator is configured for astable operation. (The internal TRIGGER signal to the oscillator is internally tied to THRESHOLD. See Figure 4.) V_{CAP} oscillates between ⅓ & ⅔ V_{DD} (or 10% & 90% if low voltage mode is selected). The delay time equations for both supply conditions are provided in the following paragraph.

Extended Delay Time Equations:

For standard supply voltages (V_{LOW} Bit = 0)

Oscillator Period (t_{OSC}) = 0.695 x (R_A+2R_B) x C_{Total}

Total Delay Time = Counter Setting (or Mult) x t_{OSC}

Total Delay Time = Mult x 0.695 x (R_A+2R_B) x C_{Total}

where $C_{Total} = C_T + C_{TI}$

C_T = External timing capacitor

C_{TI} = Internal 100pF timing capacitor

For low voltage mode (V_{LOW} Bit = 1)

Oscillator Period (t_{OSC}) = 2.197 x (R_A+2R_B) x C_{Total}

Total Delay Time = Counter Setting (or Mult) x t_{OSC}

Total Delay Time = Mult x 2.197 x (R_A+2R_B) x C_{Total}

The chart in Figure 11 shows nominal delay times for multiplier settings from 1 to 10^6 and resistor values (R_A+2R_B) from 1KΩ to 10MΩ. (The internal timing capacitor, C_{TI}, equals 100pF. No external capacitor.) The resulting delay times cover an eight-decade range!

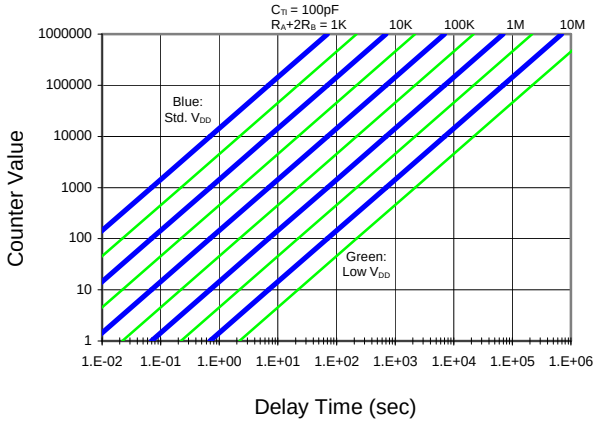


Figure 11 – Extended Period Delay Chart

The component values required for some common delay times are listed in Table 5. For this calculation, the value of R_A and R_B are equal. To keep the overall power low, values above 1MΩ were selected.

Delay	Multiplier	C_{Total} Value	R_A & R_B
1 msec	1	100pF	2.35 MΩ
1 sec.	1K	100pF	4.8 MΩ
1 min.	100K	100pF	2.9 MΩ
1 hour	1M	500pF	3.5 MΩ
1 day	1M	0.01uF	4.1 MΩ
1 week	1M	0.1uF	2.9 MΩ

Table 5 – Extended Period Delay Table

Note:

$C_{Total} = C_T + C_{TI}$

C_T = External timing capacitor (may be zero)

C_{TI} = Internal 100pF timing capacitor

Astable Operation

(Standard 555 Mode)

The circuit in Figure 12 shows the astable or "free running oscillator" configuration. If the counter setting equals one, the counter is bypassed and the device operates like a standard 555 timer. With the TRIGGER input tied to THRESHOLD, a new timing cycle is started each time V_{TH} drops below the lower comparator trip level.

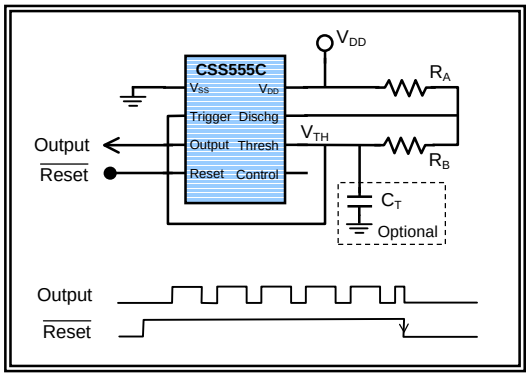


Figure 12 – Astable Circuit (Std. Mode)

The capacitor charges to ⅔ V_{DD} through (R_A+R_B) and discharges to ⅓ V_{DD} through R_B. (As in the monostable mode, the trip levels are changed to 10% & 90% for low supply voltages. This selection is made via the EEPROM.) The duty cycle is determined by the ratio of R_A and R_B. Typical signal waveforms are shown in Figure 13. The RESET input must be held high for the oscillator to be active. If RESET is brought low, the OUTPUT pin is immediately forced low and oscillation halts. Equations for the free running oscillator are provided in the following paragraph.

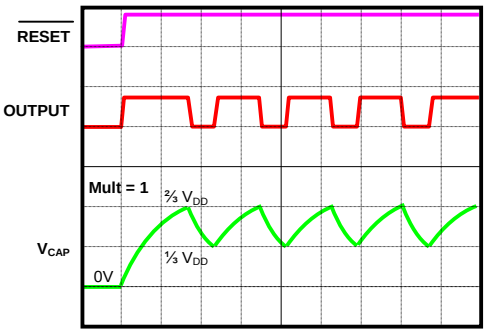


Figure 13 – Astable Waveforms (Std. Mode)

Note: The TRIGGER signal is connected to V_{TH}

Free Running Oscillator Equations:

For standard supply voltages (V_{LOW} Bit = 0)

Oscillator Period (t_{OSC}) = 0.695 x (R_A+2R_B) x C_{Total}

Osc. Freq. (f_{OSC}) = 1/t_{OSC} = 1.44/[(R_A+2R_B) x C_{Total}]

where C_{Total} = C_T + C_{TI}

C_T = External timing capacitor

C_{TI} = Internal 100pF timing capacitor

For low voltage mode (V_{LOW} Bit = 1)

Oscillator Period (t_{OSC}) = 2.197 x (R_A+2R_B) x C_{Total}

Osc. Freq. (f_{OSC}) = 1/t_{OSC} = 0.455/[(R_A+2R_B) x C_{Total}]

Duty Cycle = R_B/(R_A+2R_B)

The chart in Figure 14 shows nominal oscillator frequencies for resistor values (R_A+2R_B) from 1KΩ to 10MΩ and capacitor values from 100pF to 1uF. The resulting frequency range extends from 1 Hz to 1 MHz. (For this chart, the counter is bypassed; Mult = 1.)

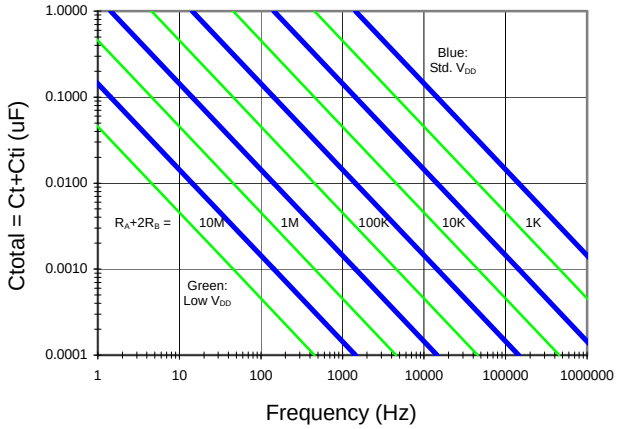


Figure 14 – Astable Frequency Chart (Std. Mode)

Astable Operation

(Extended Period or "EP" Mode)

The circuit in Figure 15 employs the internal decade counter to divide the 555 oscillator frequency by the multiplier setting. The multiplier value, 10 to 10^6, is selected by the EEPROM. The 555 analog block is configured as a free running oscillator, which supplies the input clock to the counter. The oscillator runs when RESET is high (logic one) and TRIGGER is low. Each divide by 10 stage of the decade counter consists of a divide by 5 followed by a divide by 2. This configuration provides a 50% output duty cycle no matter which multiplier setting is selected. Waveforms for this mode are shown in Figure 16.

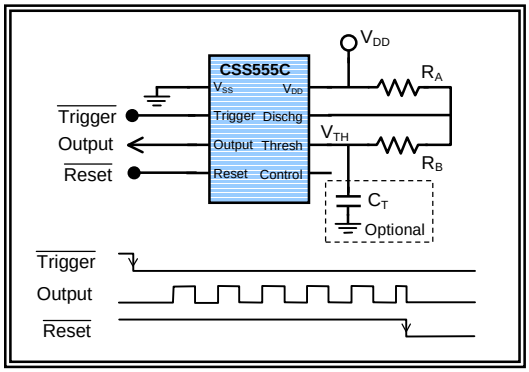


Figure 15 – Astable Circuit (EP Mode)

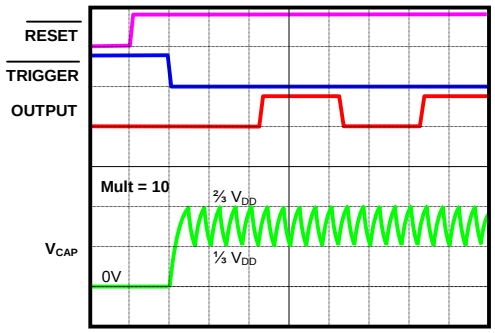


Figure 16 – Astable Waveforms (EP Mode)

Free Running Oscillator Equations:

For standard supply voltages (V_{LOW} Bit = 0)

Oscillator Period (t_{OSC}) = 0.695 x (R_A+2R_B) x C_{Total}

Osc. Freq. (f_{OSC}) = 1/t_{OSC} = 1.44/[(R_A+2R_B) x C_{Total}]

Output Frequency = f_{OSC}/Mult

where C_{Total} = C_T + C_{TI}

C_T = External timing capacitor

C_{TI} = Internal 100pF timing capacitor

For low voltage mode (V_{LOW} Bit = 1)

Oscillator Period (t_{OSC}) = 2.197 x (R_A+2R_B) x C_{Total}

Osc. Freq. (f_{OSC}) = 1/t_{OSC} = 0.455/[(R_A+2R_B) x C_{Total}]

Output Frequency = f_{OSC}/Mult

Duty Cycle = 50%

The chart in Figure 17 shows nominal oscillator frequencies for multiplier settings from 1 to 10^6 and resistor values (R_A+2R_B) from 1KΩ to 10MΩ. (The internal timing capacitor, C_{TI}, equals 100pF. No external timing capacitor.) The resulting frequencies range from less than 1Hz to 1MHz.

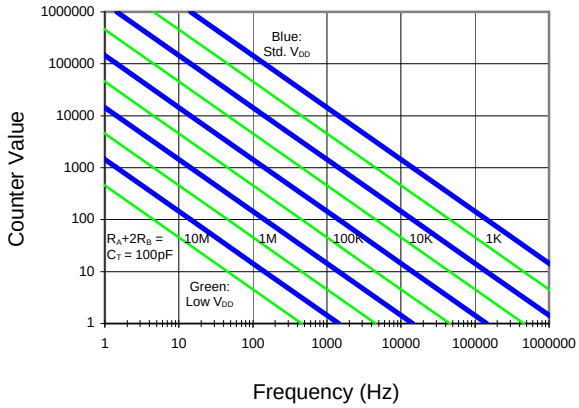


Figure 17 – Astable Frequency Chart (EP Mode)

EEPROM (Configuration Memory)

An internal EEPROM provides two bytes of nonvolatile memory that stores the configuration information and the 100pF capacitor trim setting. The configuration bits control the multiplier setting (1 to 10^6), the power setting (micro or low) and the comparator trip levels (standard or low voltage). (See Tables 1A & 1B for more details.) By employing an internal EEPROM for configuration control, the pin count and pin functions remain compatible with existing 555 IC's.

The EEPROM includes a high voltage generator. No special signal levels are required to Read or Write to it. Access to the EEPROM is enabled by forcing the CONTROL pin to GND. (This pin is normally left open and an internal voltage divider holds it at ⅔V_{DD}.) With CONTROL held at GND, the TRIGGER and RESET pins are redefined to be SCLK (Serial Clock) and SDIN (Serial Data In). Data from the EEPROM can be read at the OUTPUT pin. The interface is simple and straightforward. It can support programming individual units or devices installed in their application circuit. A detailed description of the serial interface is provided in Application Note AN555-1 ("CSS555C EEPROM Serial Interface"). A development kit is available and provides both programming and evaluation capabilities. It uses a standard PC and one USB port. Please contact Custom Silicon Solutions for more information.

The core EEPROM cell is a differential, floating gate circuit. Like an SRAM, it features zero static current. Its output data is valid whenever the supply voltage is above 1.0V. It has excellent data retention and endurance characteristics. Data retention is greater than 10 years at 85℃ and its endurance (maximum number of Store cycles) is greater than 100,000 cycles. A typical Store operation can be performed in less than 25 msec.

Supply Current Considerations

The internal supply current used by the CSS555C can be divided into three main components:

1) ~ 1.8uA constant current (independent of V_{DD})
2) ~ 6 MΩ from V_{DD} to GND (0.5uA at V_{DD} = 3V)
3) ~ 0.5uA switching current at V_{DD} = 3V, F_{OSC} = 100KHz (~ linearly proportional to V_{DD} & F_{OSC})

To minimize the second component, keep V_{DD} as low as possible. To minimize the switching current, keep V_{DD} & F_{OSC} low. (Choose a lower multiplier value so the oscillator frequency is well below 100 KHz.)

The external current is determined by the values of R_A and R_B. They should be as high as practical. (PCB surface leakage typically limits the value to ≤10MΩ.)

The CSS555C has a "Break-Before-Make" driver for the OUTPUT signal. This circuit eliminates the large "through current" that flows directly from V_{DD} to GND during each output transition. This significantly reduces the noise injected into the power supply. The discharge path in the monostable configuration is another source of transient current. (When V_{TH} reaches the upper trip point, the capacitor is very quickly discharged to GND.) To minimize this transient current, simply add a resistor (R_{LIM}) in series with the DISCHARGE pin. (see Figure 18) The value of R_{LIM} must be low enough to allow the timing capacitor to completely discharge before the next timing cycle. A typical value for R_{LIM} is 1KΩ to 10KΩ.

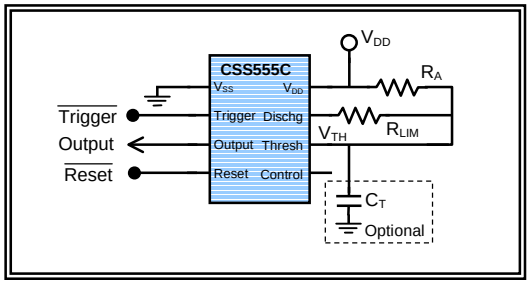


Figure 18 – Monostable with R_{LIM}

ESD Protection

All input and output pins include protection devices to guard against ESD damage. A simplified schematic of the input protection circuit is shown in Figure 19. The voltage levels at all pins should be kept between (V_{SS} – 0.3V) and (V_{DD} +0.3V) to prevent forward biasing the diodes.

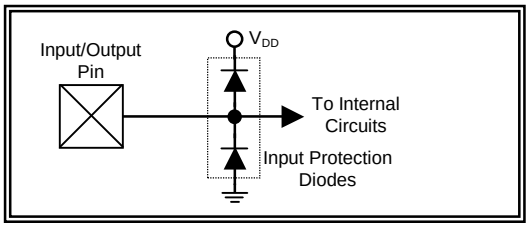


Figure 19 – Input Protection Circuit

Internal Timing Capacitor

The internal timing capacitor is a Poly/Poly structure which has excellent stability over temperature (TC ~ 25 ppm/℃) and voltage (VC ~ 250 ppm/V). It consists of a fixed 75pF capacitor (C_{TIB}) and a 0pF to 40pF trim capacitor (C_{TIA}). Eight EEPROM bits store the trim setting with a step size of ~ 0.16pF. The value is set at final package test, but may be re-adjusted by the user. (See application note AN555-1 for more details.) The third capacitor, C_S, is the stray capacitance due to the pad cell, bond wire and package leadframe. It is typically 5pF.

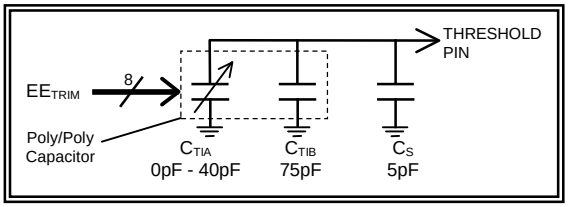


Figure 20 – Internal 100pF Timing Capacitor

Ordering Information

Part Number	Package Description	Shipping Options
CSS555C-ID	8 pin plastic DIP	50 units / Rail
CSS555C-IS	8 pin plastic SOIC	98 units / Rail
CSS555C-ISTR	8 pin plastic SOIC	2500 units / Tape & Reel
CSS555C_IW	Die or Tested Wafers	Contact CSS for options
CSS555C_DVK	Development Kit	N.A.

Table 6 – Ordering Options

All packaging options use lead free materials. All part types are rated for operation from -40℃ to +85℃.

The default configuration stored in EEPROM is:

Configuration Data =	80_{HEX}
Operating Mode =	Standard 555
Power Setting =	Micro
Voltage Setting =	Standard
Timing Capacitor =	Trimmed to 100pF

Packaged parts may be ordered with alternate configuration settings. A minimum purchase and/or service charge may apply. Please contact CSS for details.

Development Kit

The "CSS555C Development Kit" is a PC based system that allows the user to Read and Program the internal EEPROM. It includes an easy to use dialog box and serial interface (USB port required). The circuit card includes plenty of extra terminals so that most applications can be built and evaluated quickly and easily. For more information, please refer to the development kit's instruction manual.

Typical Performance Characteristics

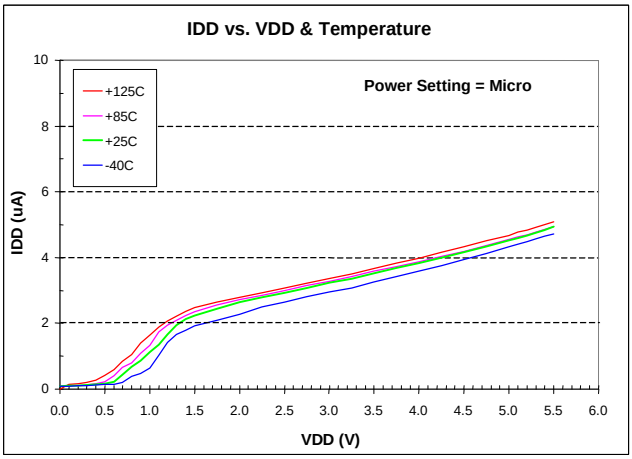


Figure 21 Supply Current (Micro Power)

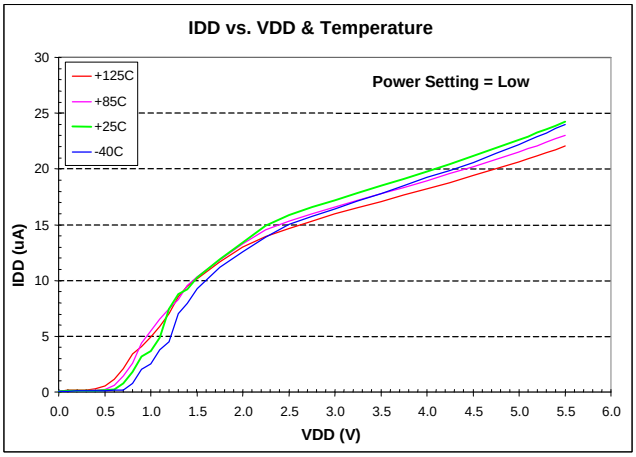


Figure 22 Supply Current (Low Power)

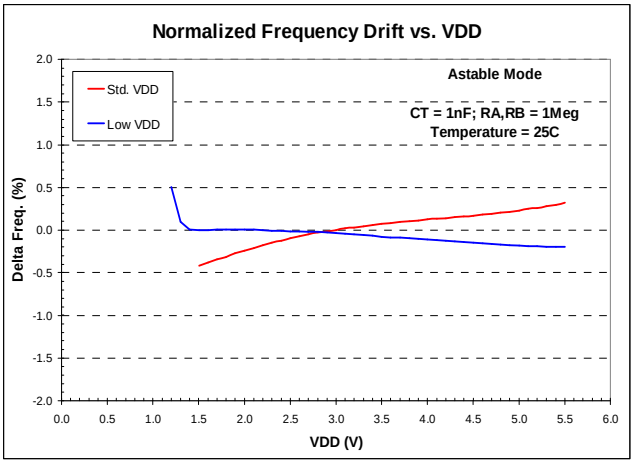


Figure 23 Frequency Drift vs. V_{DD}

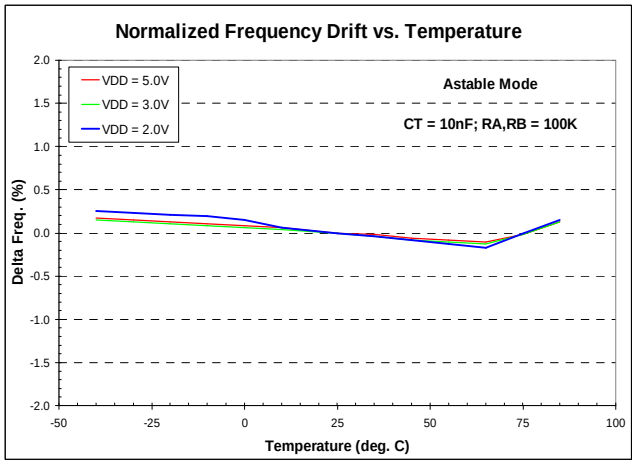


Figure 24 Frequency Drift vs. Temperature

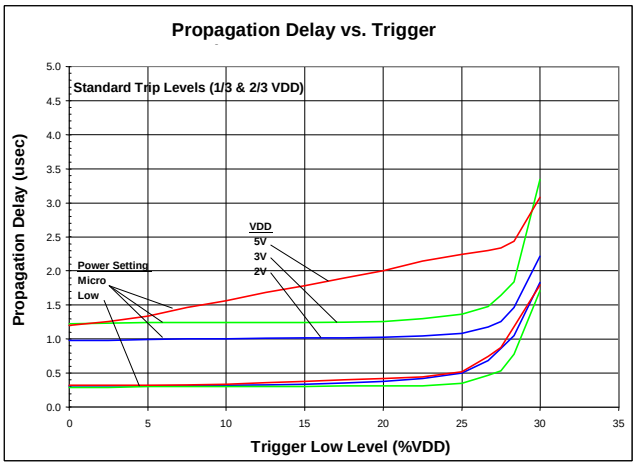


Figure 25 Propagation Delay (Standard V_{DD})

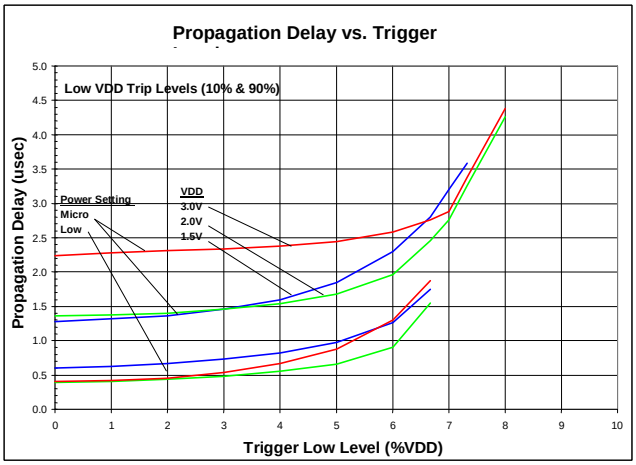


Figure 26 Propagation Delay (Low V_{DD})

Typical Performance Characteristics (continued)

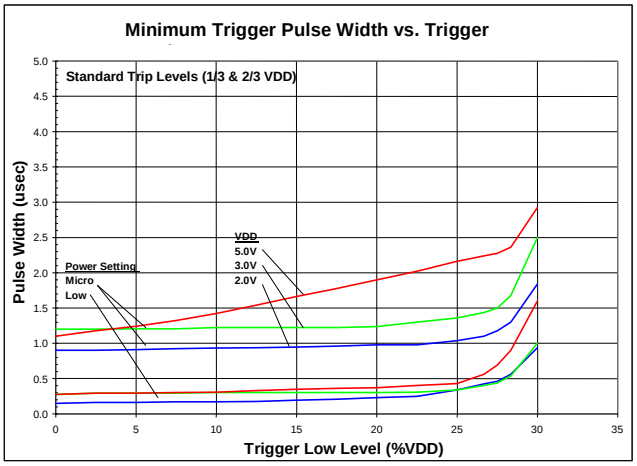


Figure 27 Trigger Pulse Width (Std. V_{DD})

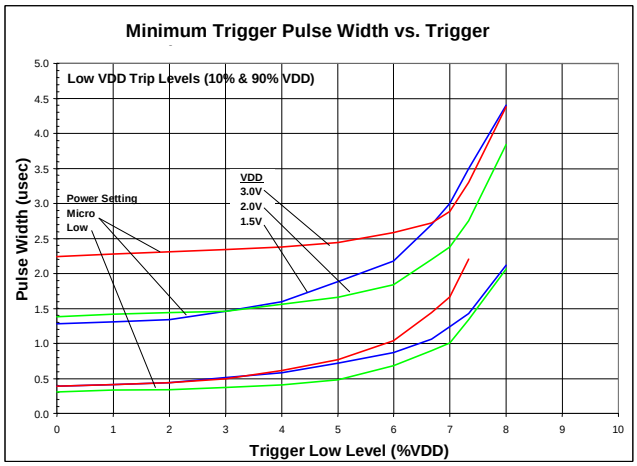


Figure 28 Trigger Pulse Width (Low V_{DD})

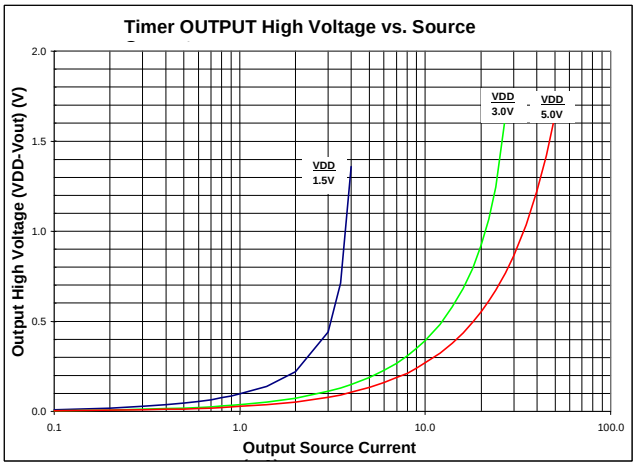


Figure 29 OUTPUT V_{OH} vs. I_{OH}

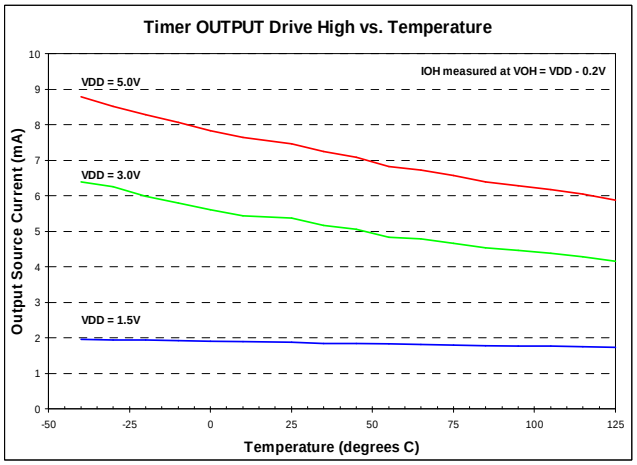


Figure 30 OUTPUT I_{OH} vs. Temperature

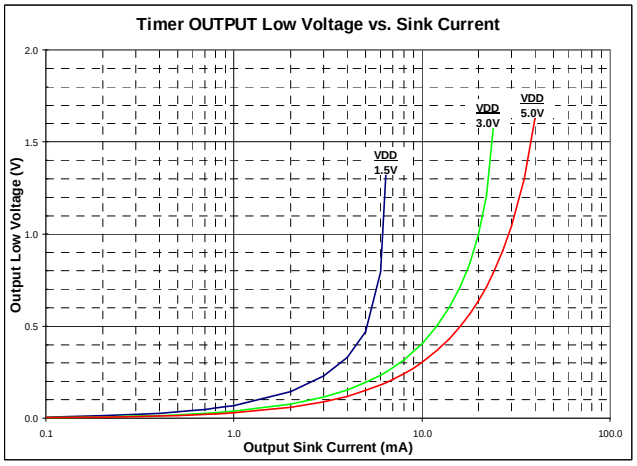


Figure 31 OUTPUT V_{OL} vs. I_{OL}

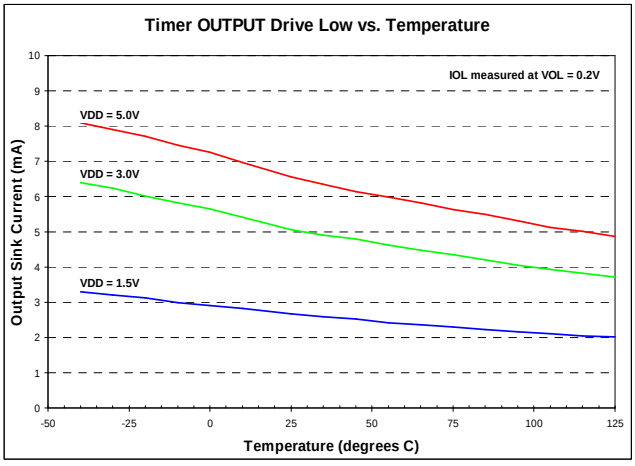


Figure 32 OUTPUT I_{OL} vs. Temperature

Typical Performance Characteristics (continued)

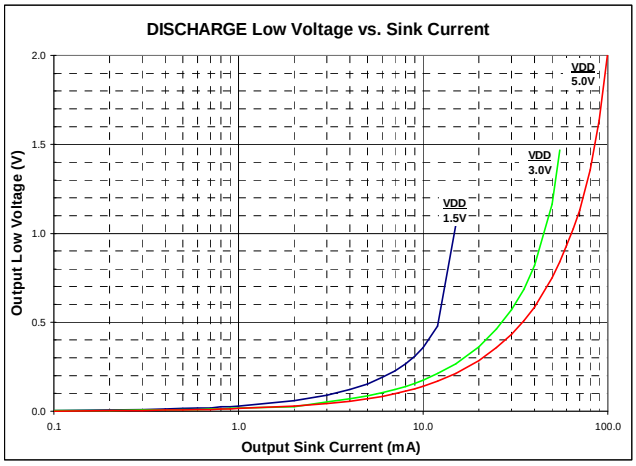


Figure 33 DISCHARGE V_{OL} vs. I_{OL}

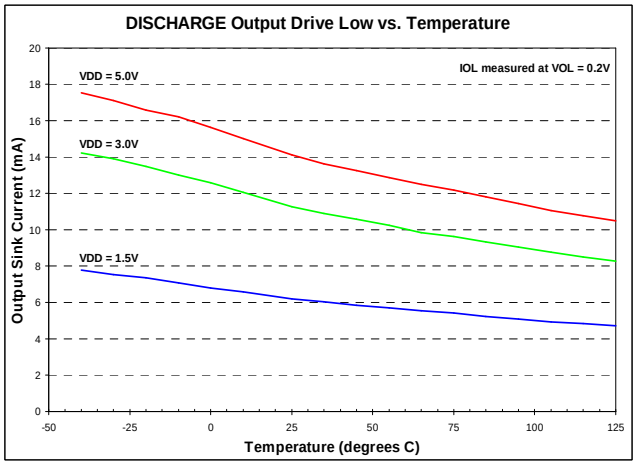


Figure 34 DISCHARGE I_{OL} vs. Temperature

PACKAGE DRAWINGS

Pinout Diagram

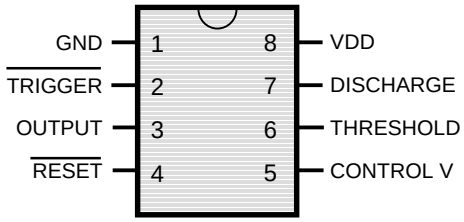


Figure 35

SOIC Dimensions				
	Inches		Millimeters	
Symbol	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Table 7

SOIC Mechanical Drawing

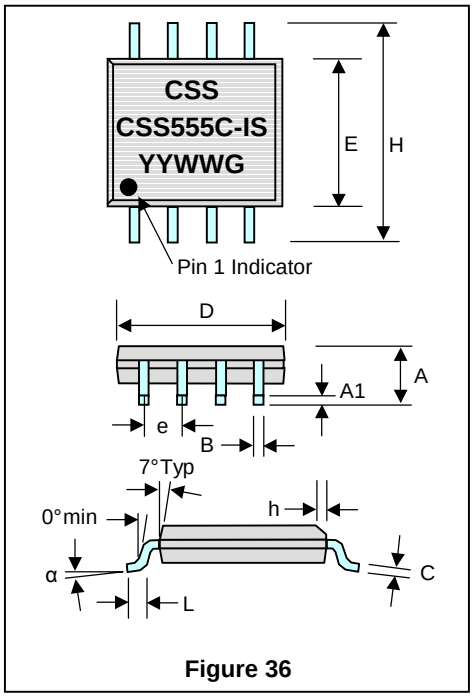


Figure 36

PDIP Dimensions				
	Inches		Millimeters	
Symbol	MIN	MAX	MIN	MAX
A1	0.015	-	0.38	-
A2	0.128	0.132	3.25	3.35
b	0.014	0.022	0.36	0.56
b2	0.057	0.068	1.45	1.73
b3	0.032	0.046	0.81	1.17
C	0.010	0.012	0.25	0.30
D	0.375	0.385	9.53	9.78
E	0.300	0.320	7.62	8.13
E1	0.245	0.255	6.22	6.48
e	0.100		2.54	
eB	0.330	0.370	8.38	9.40
Q1	0.055	0.080	1.40	2.03
S	0.025	0.080	0.06	2.03
α	3°	8°	3°	8°

Table 8

PDIP Mechanical Drawing

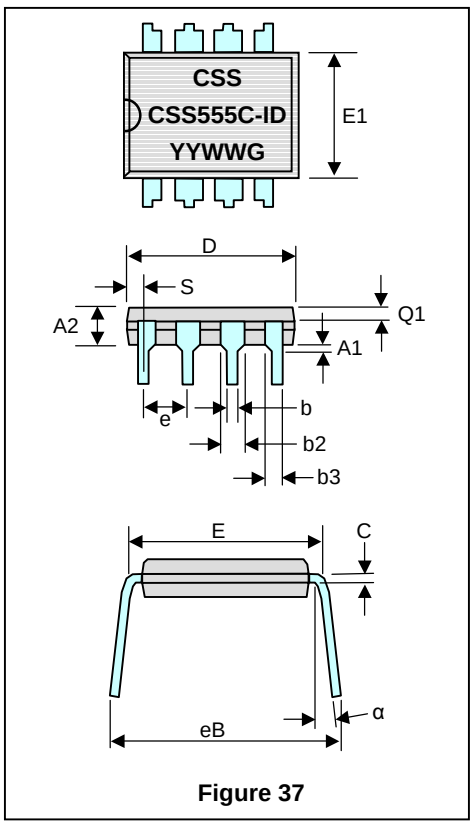


Figure 37