

## CMOS Hex Buffer

### High-Voltage Types (20-Volt Rating)

#### 3-State Non-Inverting Type

- CD4503B is a hex noninverting buffer with 3-state outputs having high sink- and source-current capability. Two disable controls are provided, one of which controls four buffers and the other controls the remaining two buffers.

The CD4503B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

#### Features:

- 1 TTL-load output drive capability
- 2 output-disable controls
- 3-state outputs
- Pin compatible with industry types MM80C97, MC14503, and 340097
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and  $25^\circ\text{C}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

#### Applications:

- 3-state hex buffer for interfacing IC's with data buses
- CMOS to TTL hex buffer

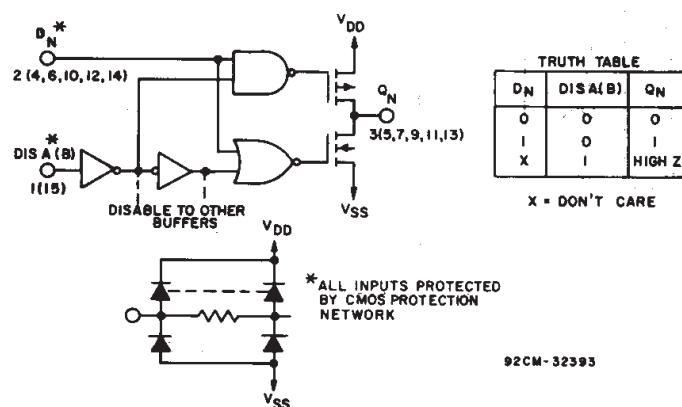


Fig. 1—Logic diagram of 1 to 6 identical buffers.

#### MAXIMUM RATINGS, Absolute-Maximum Values:

##### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) .....  $-0.5\text{V}$  to  $+20\text{V}$

INPUT VOLTAGE RANGE, ALL INPUTS .....  $-0.5\text{V}$  to  $V_{DD} + 0.5\text{V}$

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10\text{mA}$

##### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  .....  $500\text{mW}$

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at  $12\text{mW}/^\circ\text{C}$  to  $200\text{mW}$

##### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

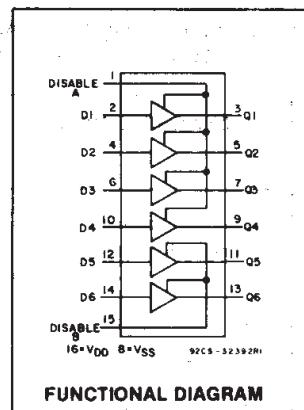
FOR  $T_A =$  FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .....  $100\text{mW}$

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

##### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79\text{mm}$ ) from case for  $10\text{s}$  max .....  $+265^\circ\text{C}$



FUNCTIONAL DIAGRAM

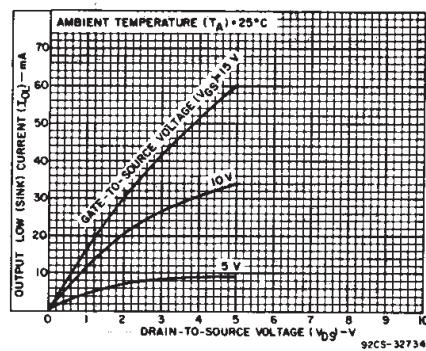


Fig. 2—Typical n-channel output low (sink) current characteristics.

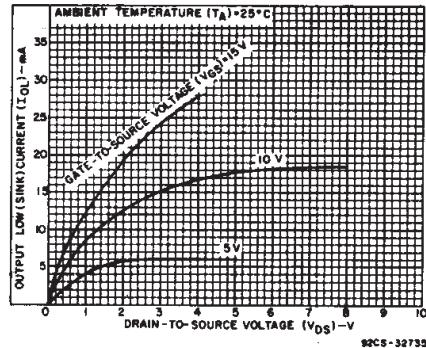
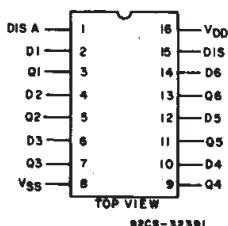


Fig. 3—Minimum n-channel output low (sink) current characteristics.



## TERMINAL ASSIGNMENT

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			
Quiescent Device	—	0.5	5	1	1	30	30	—	0.02	1	μA
Current, $I_{DD}$ Max.	—	0.10	10	2	2	60	60	—	0.02	2	μA
Current, $I_{DD}$ Max.	—	0.15	15	4	4	120	120	—	0.02	4	μA
Current, $I_{DD}$ Max.	—	0.20	20	20	20	600	600	—	0.04	20	μA
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0	5	2.6	2.5	1.4	1.3	2.1	2.3	—	mA
Output High (Source) Current, $I_{OH}$ Min.	0.5	0	10	6.5	6.4	3.9	3.8	5.5	6.2	—	mA
Output High (Source) Current, $I_{OH}$ Min.	1.5	0	15	19.2	18.9	11.4	11.2	16.1	23	—	mA
Output Voltage: Low- Level, $V_{OL}$ Max.	—	0.5	5	0.05				—	0	0.05	V
Output Voltage: High- Level, $V_{OH}$ Min.	—	0.10	10	0.05				—	0	0.05	V
Output Voltage: High- Level, $V_{OH}$ Min.	—	0.15	15	0.05				—	0	0.05	V
Input Low Voltage, $V_{IL}$ Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
Input Low Voltage, $V_{IL}$ Max.	1.9	—	10	3				—	—	3	V
Input Low Voltage, $V_{IL}$ Max.	1.5, 13.5	—	15	4				—	—	4	V
Input High Voltage, $V_{IH}$ Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
Input High Voltage, $V_{IH}$ Min.	1.9	—	10	7				7	—	—	V
Input High Voltage, $V_{IH}$ Min.	1.5, 13.5	—	15	11				11	—	—	V
Input Current $I_{IN}$ Max.	—	0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	—	$\pm 10^{-5}$	$\pm 0.1$	μA
3-State Output Leakage Current, $I_{OUT}$ Max.	0.18	0.18	18	$\pm 0.4$	$\pm 0.4$	$\pm 12$	$\pm 12$	—	$\pm 10^{-4}$	$\pm 0.4$	μA

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS			UNITS
	Min.	Max.		
Supply-Voltage Range (For $T_A$ = Full Package- Temperature Range)	3	18		V

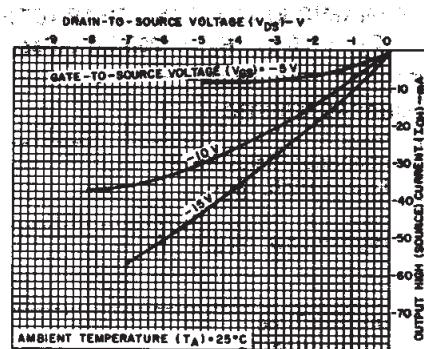


Fig. 4—Typical p-channel output high (source) current characteristics.

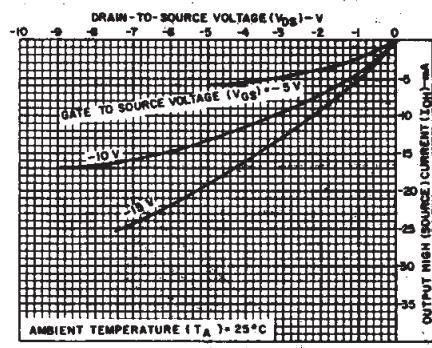


Fig. 5—Minimum p-channel output high (source) current characteristics.

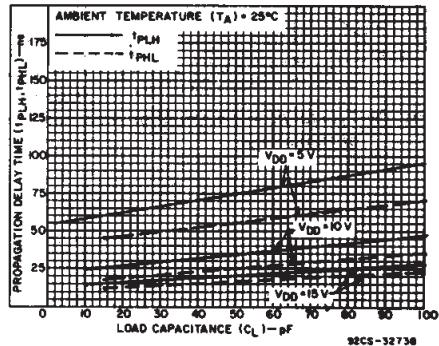


Fig. 6—Typical propagation delay time as a function of load capacitance.

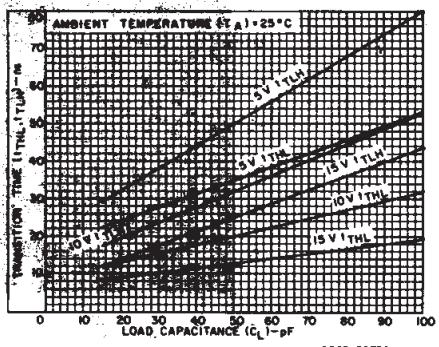


Fig. 7—Typical transition time as a function of load capacitance.

## CD4503B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$  unless otherwise specified.

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		Typ.	Max.	
Propagation Delay Time: Low-to-High, $t_{PLH}$	5	75	150	ns
	10	35	70	
	15	25	50	
High-to-Low, $t_{PHL}$	5	55	110	ns
	10	25	50	
	15	17	35	
Transition Time: Low-to-High, $t_{TLH}$	5	50	90	ns
	10	30	45	
	15	25	35	
High-to-Low, $t_{THL}$	5	35	70	ns
	10	20	40	
	15	13	25	
3-State Propagation Delay Time: $R_L = 1\text{ k}\Omega$ $t_{PHZ}, t_{PZH}$	5	70	140	ns
	10	30	60	
	15	25	50	
$t_{PZL}, t_{PLZ}$	5	90	180	ns
	10	40	80	
	15	35	70	

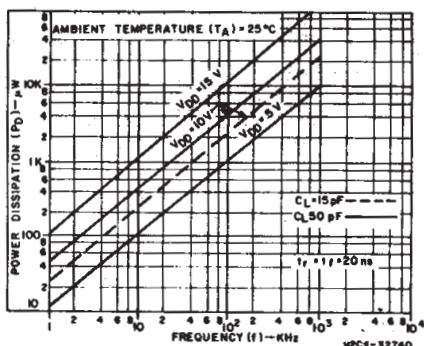


Fig. 8—Typical power dissipation as a function of frequency.

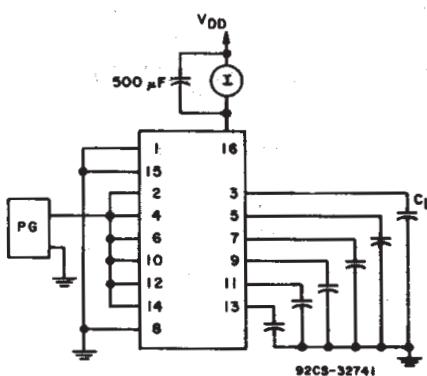


Fig. 9—Dynamic power dissipation test circuit.

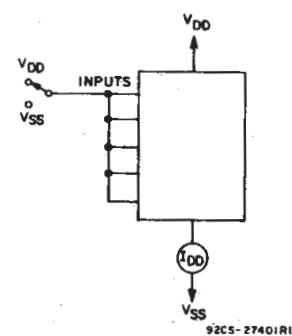


Fig. 10—Quiescent-device-current test circuit.

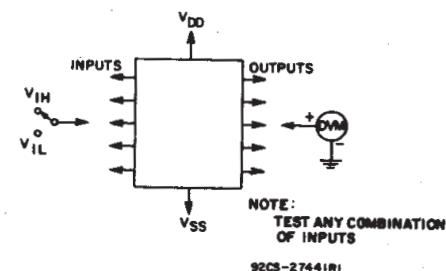


Fig. 11—Input-voltage test circuit.

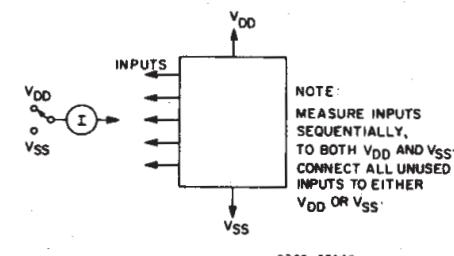
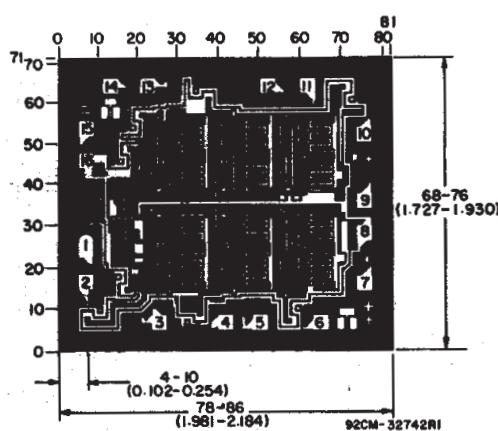


Fig. 12—Input current test circuit.



Dimensions and pad layout for CD4503BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4503BE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4503BE	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BEE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4503BE	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4503BF	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4503BF3A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4503BM	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4503BM	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4503B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM503B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD4503BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM503B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

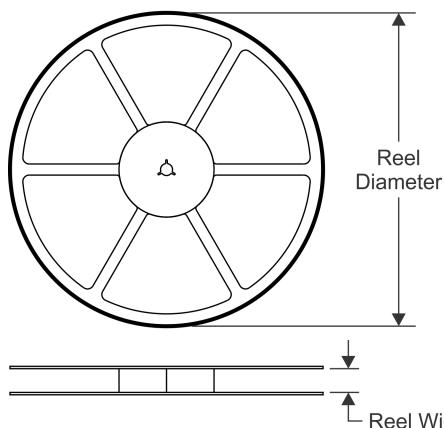
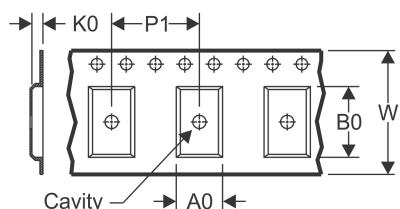
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4503B, CD4503B-MIL :**

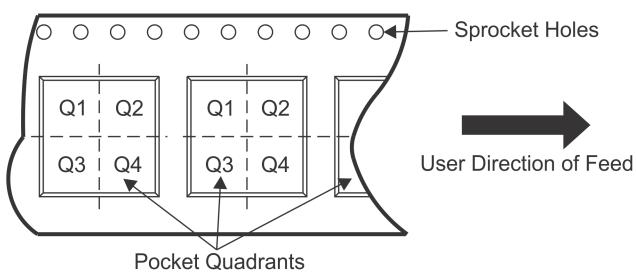
- Catalog: [CD4503B](#)
- Military: [CD4503B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

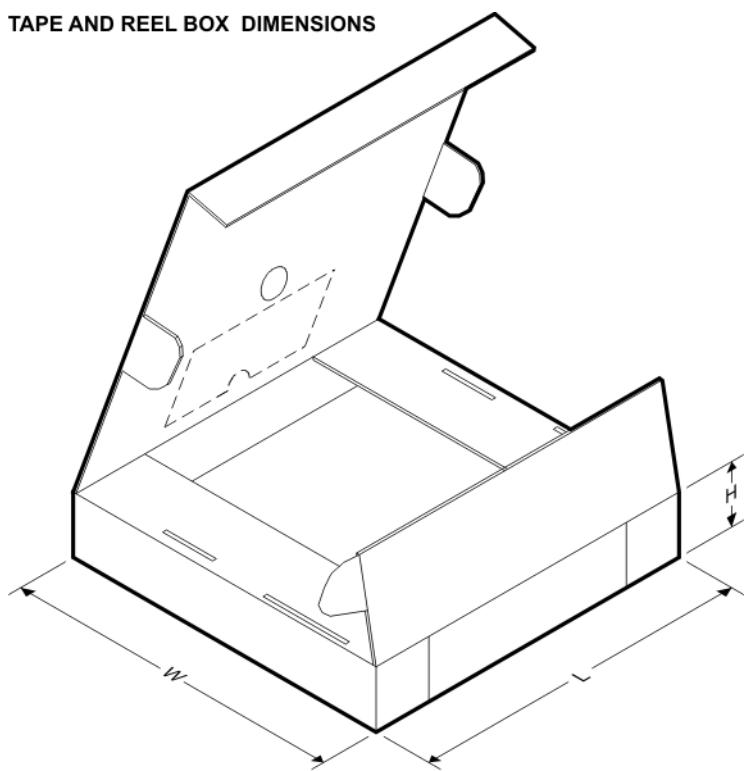
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4503BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4503BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4503BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


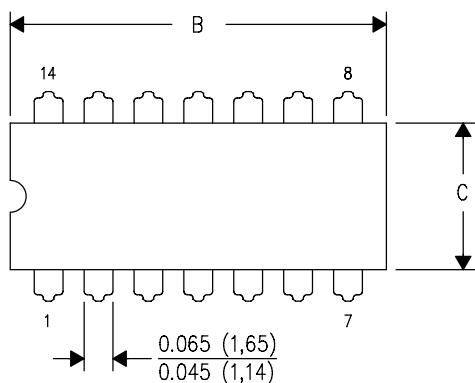
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4503BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4503BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4503BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

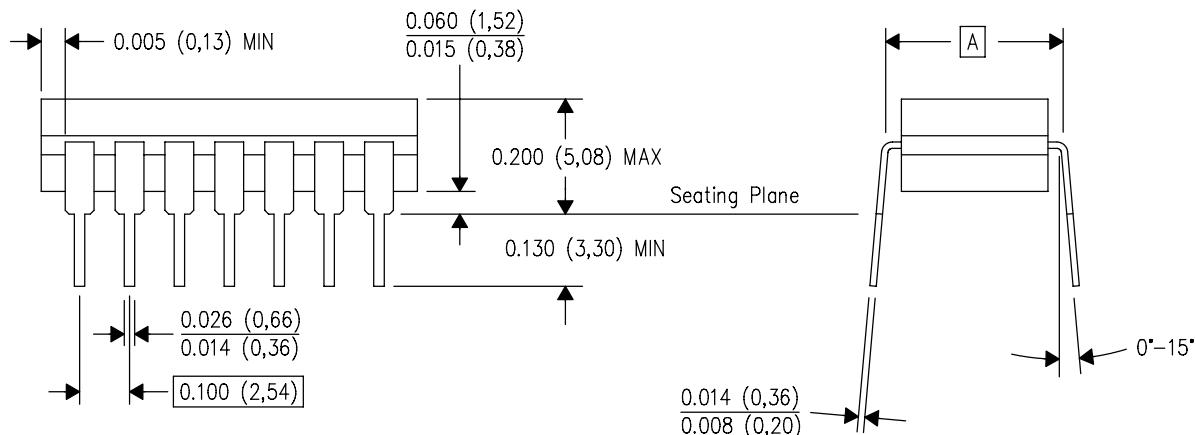
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



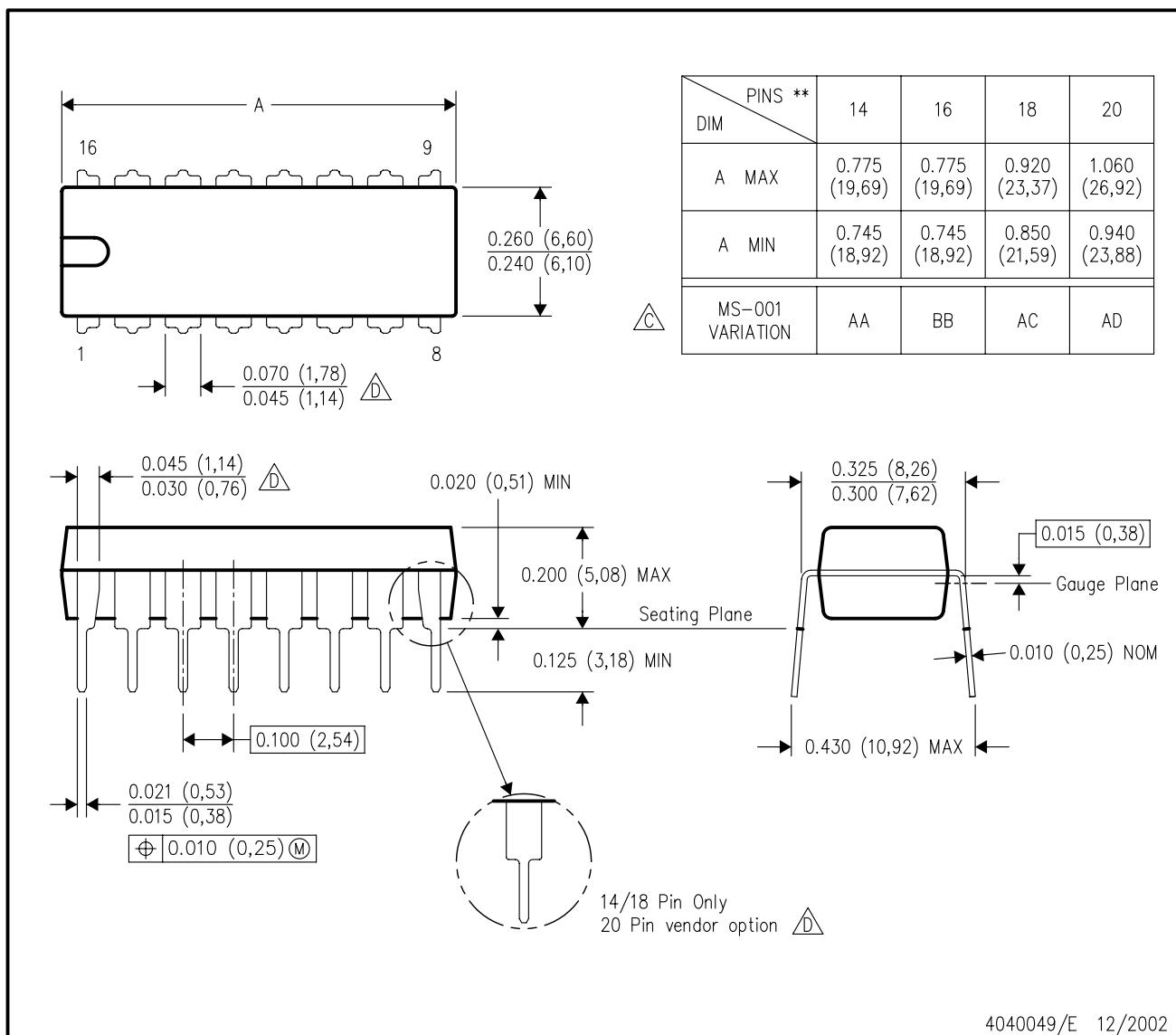
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



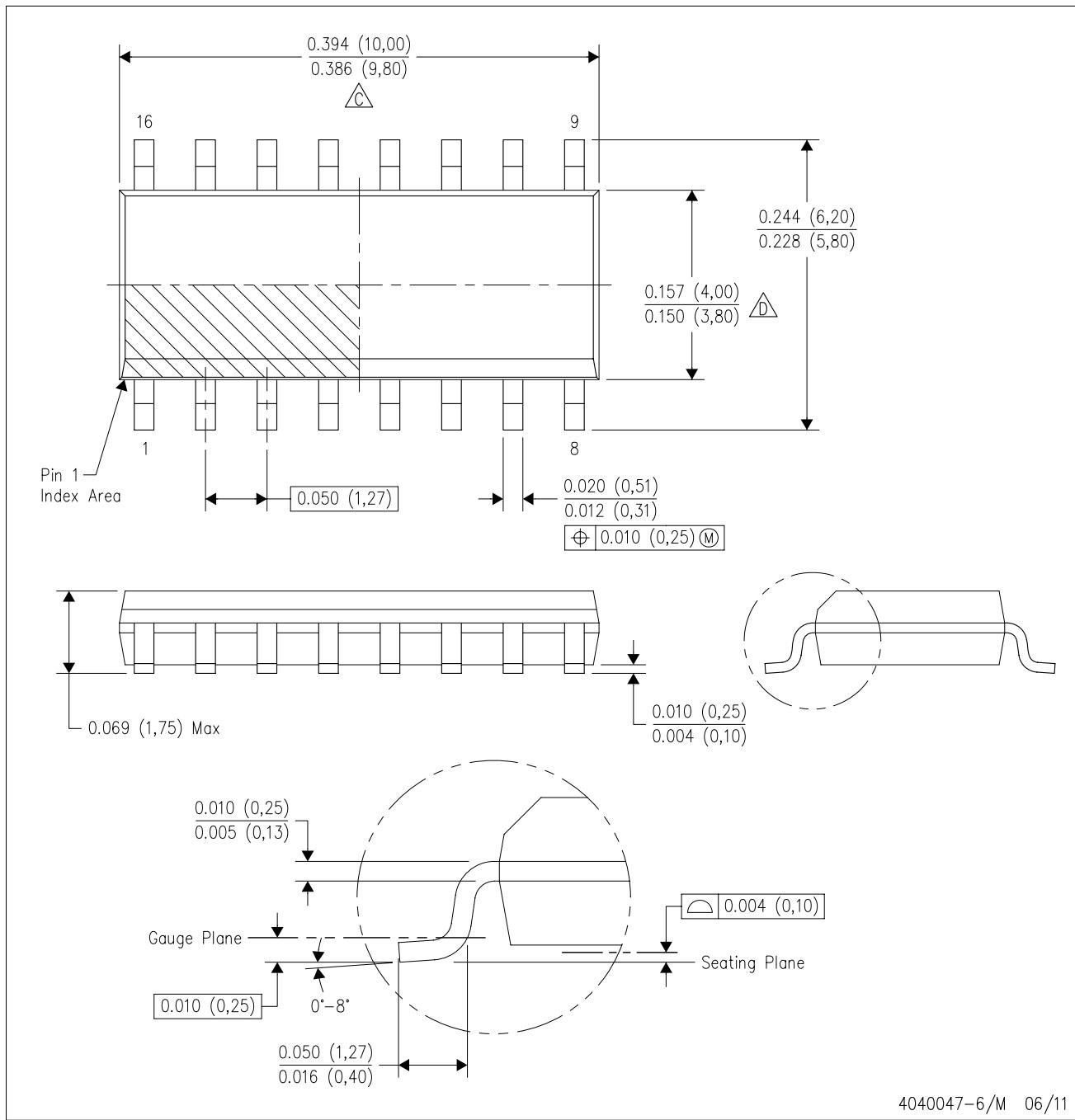
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

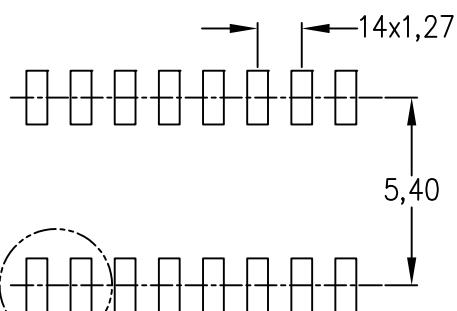
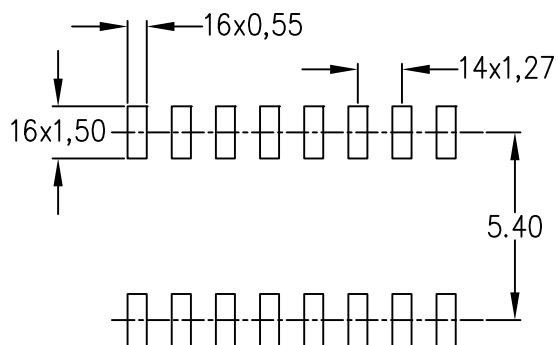
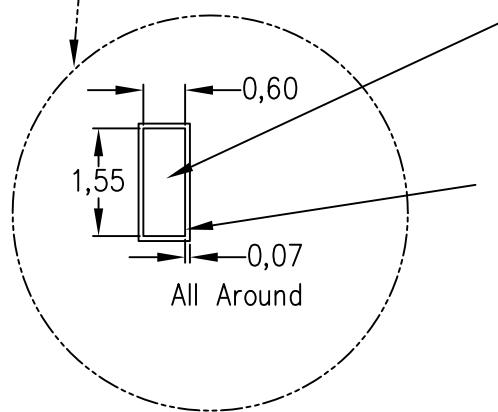
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

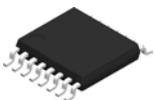
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

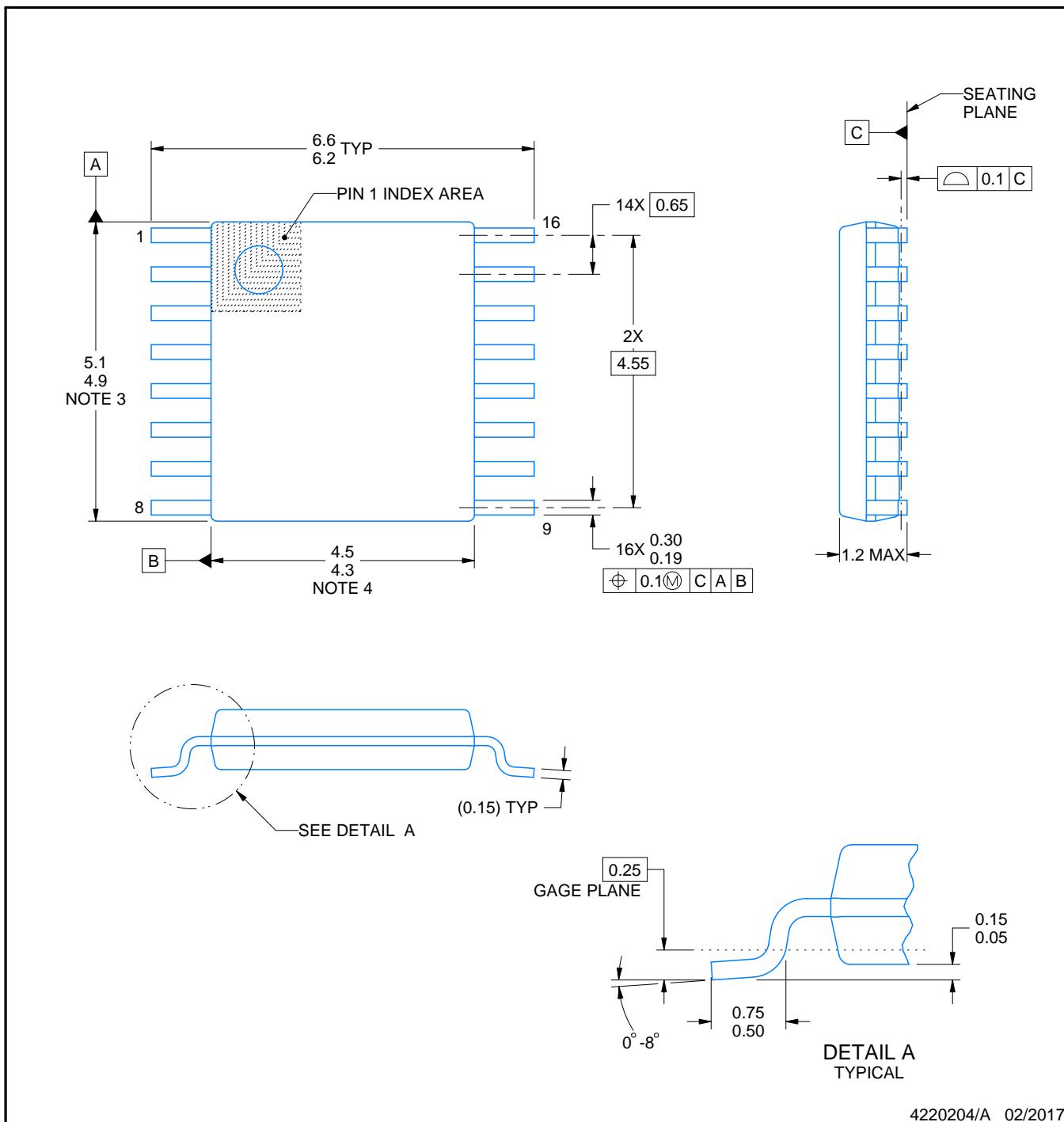
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

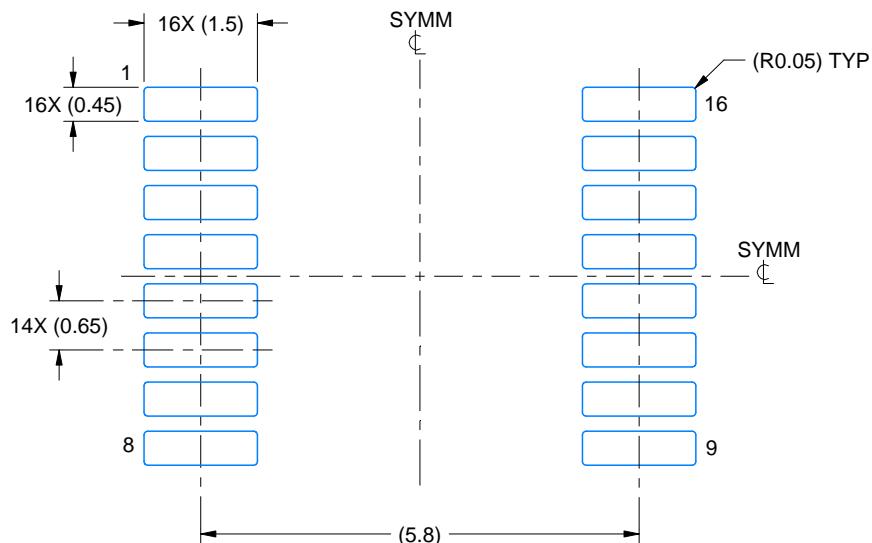
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

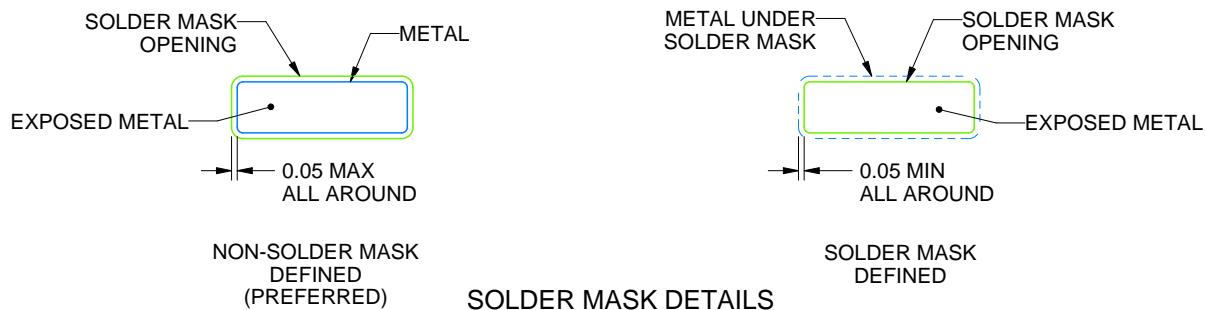
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

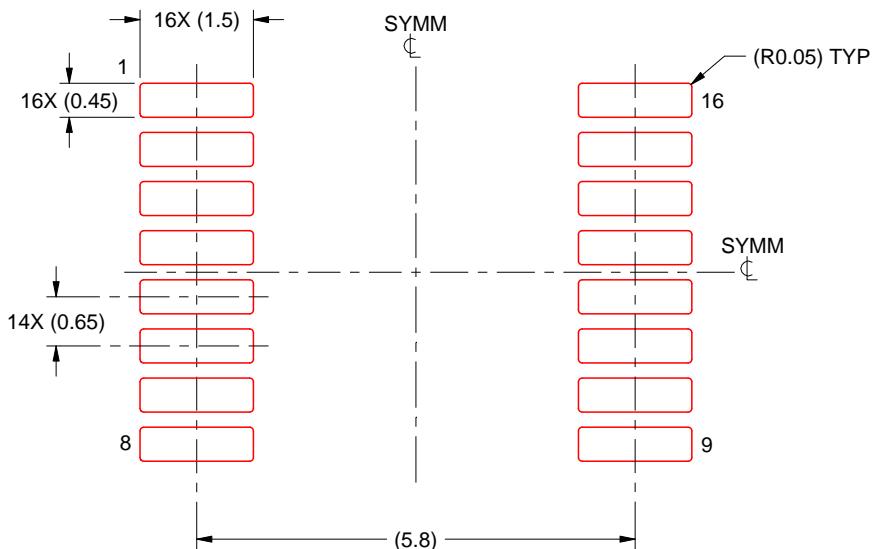
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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