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Jameco Part Number 12992TI

CD4043B, CD4044B Types

CMOS Quad 3-State R/S Latches

High-Voltage Types (20-Volt Rating)

Quad NOR R/S Latch – CD4043B

Quad NAND R/S Latch – CD4044B

■ CD4043B types are quad cross-coupled 3-state CMOS NOR latches and the CD4044B types are quad cross-coupled 3-state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs.

The CD4043B and CD4044B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (D, DR, DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

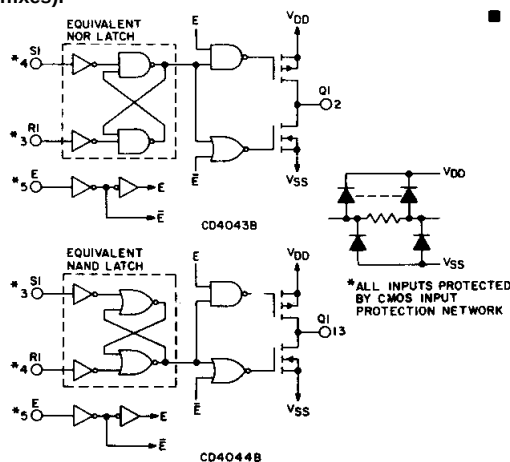


Fig. 1 – Logic diagrams.

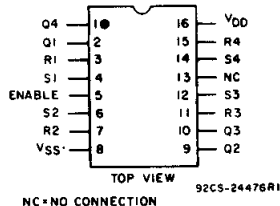
Features:

- 3-state outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V

- Meets all requirements of JEDEC Tentative Standard No. 18B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Holding register in multi-register system
- Four bits of independent storage with output ENABLE
- Strobed register
- General digital logic
- CD4043B for positive logic systems
- CD4044B for negative logic systems



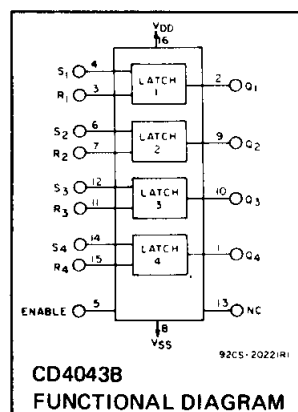
CD4043B

TERMINAL ASSIGNMENTS

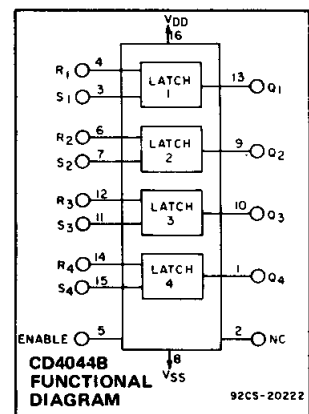
S	R	E	Q
X	X	0	OC*
0	0	1	NC*
1	0	1	1
0	1	1	0
1	1	1	Δ

* OPEN CIRCUIT
+ NO CHANGE
 Δ DOMINATED BY S=1 INPUT

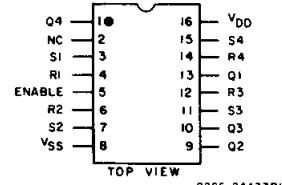
CD4043B



CD4043B
FUNCTIONAL DIAGRAM



CD4044B
FUNCTIONAL DIAGRAM



CD4044B

S	R	E	Q
X	X	0	OC*
1	1	1	NC*
0	1	1	1
1	0	1	0
0	0	1	Δ

* OPEN CIRCUIT
+ NO CHANGE
 Δ DOMINATED BY R=0 INPUT

CD4044B

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max $+265^\circ\text{C}$

TRUTH TABLES

Recommended Operating Conditions $T_A = 25^\circ\text{C}$
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range ($T_A = \text{Full Package Temperature Range}$)	—	3	18	V
SET or RESET Pulse Width, t_W	5 10 15	160 80 40	—	ns

CD4043B, CD4044B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5, 3.5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
3-State Output Leakage Current I _{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 ⁻⁴	±0.4	μA

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

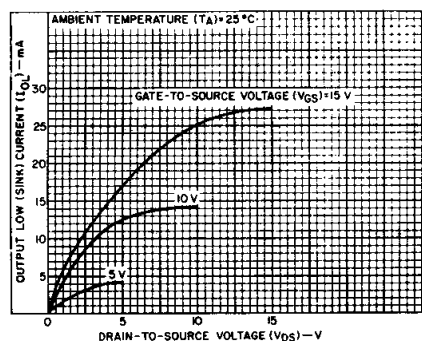


Fig. 2 — Typical output low (sink) current characteristics.

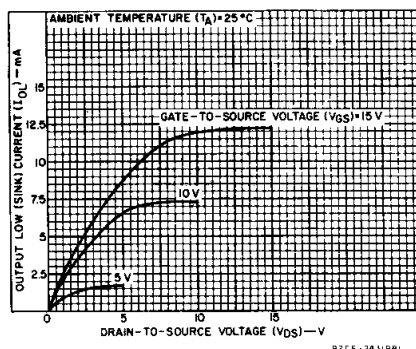


Fig. 3 — Minimum output low (sink) current characteristics.

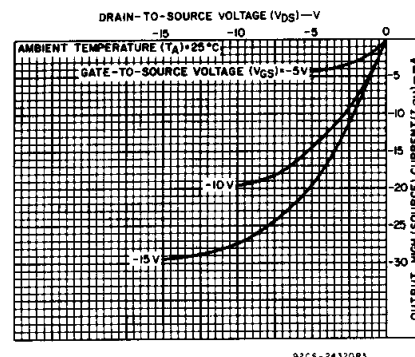


Fig. 4 — Typical output high (source) current characteristics.

CD4043B, CD4044B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES		UNITS
		TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5 10 15	150 70 50	300 140 100	ns
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5 10 15	115 55 40	230 110 80	ns
t_{PLZ}, t_{PZL}	5 10 15	90 50 35	180 100 70	ns
Transition Time: t_{THL}, t_{TLH}	5 10 15	100 50 40	200 100 80	ns
Minimum SET or RESET Pulse Width, t_W	5 10 15	80 40 20	160 80 40	ns
Input Capacitance, (Any Input) C_{IN}	—	5	7.5	pF

TEST CIRCUITS

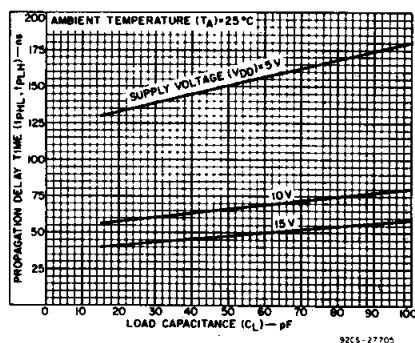


Fig. 7 — Typical propagation delay time vs. load capacitance—SET, RESET to Q, $\bar{Q}$.

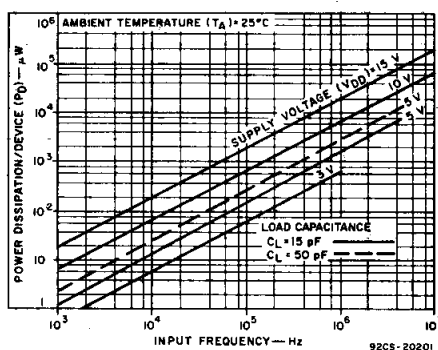


Fig. 8 — Typical power dissipation vs. frequency.

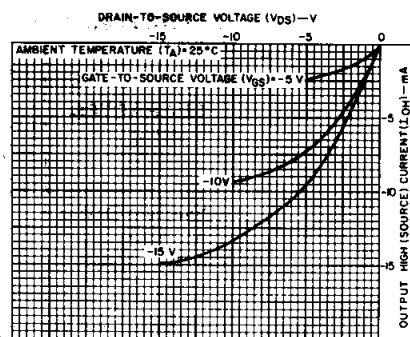


Fig. 5 — Minimum output high (source) current characteristics.

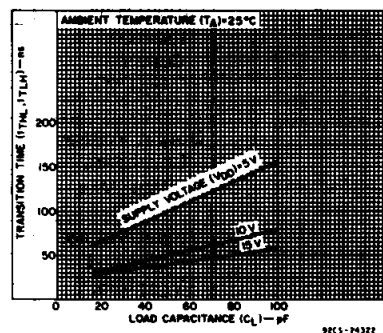


Fig. 6 — Typical transition time vs. load capacitance.

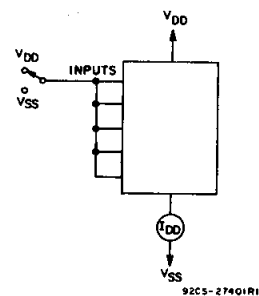


Fig. 9 — Quiescent device current.

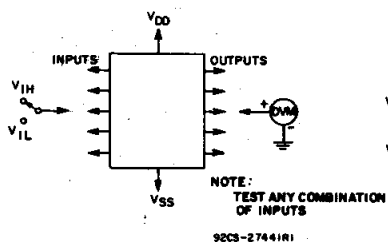


Fig. 10 — Input voltage.

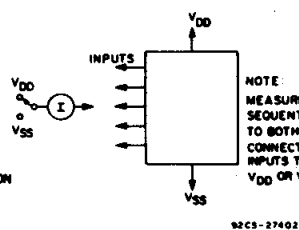


Fig. 11 — Input current.

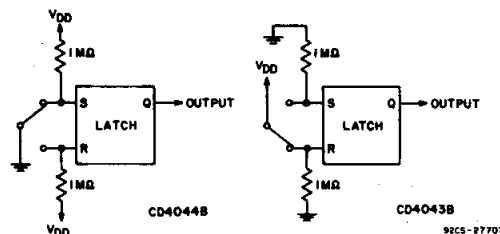


Fig. 12 — Switch bounce eliminator.

CD4043B, CD4044B Types

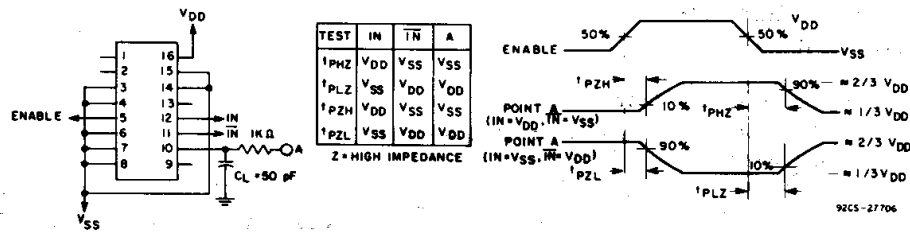
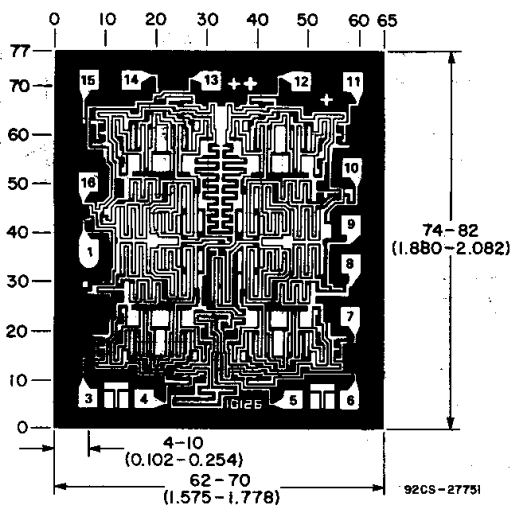
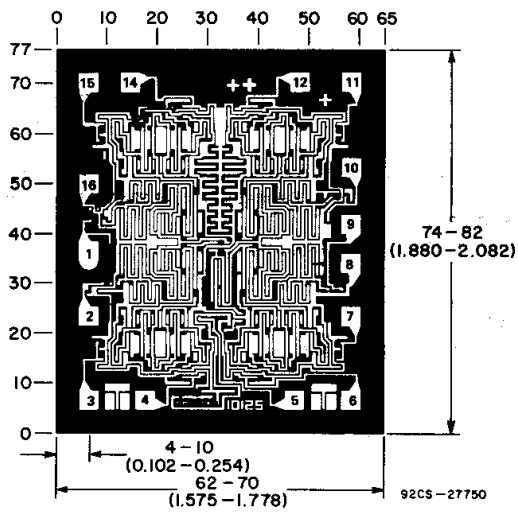
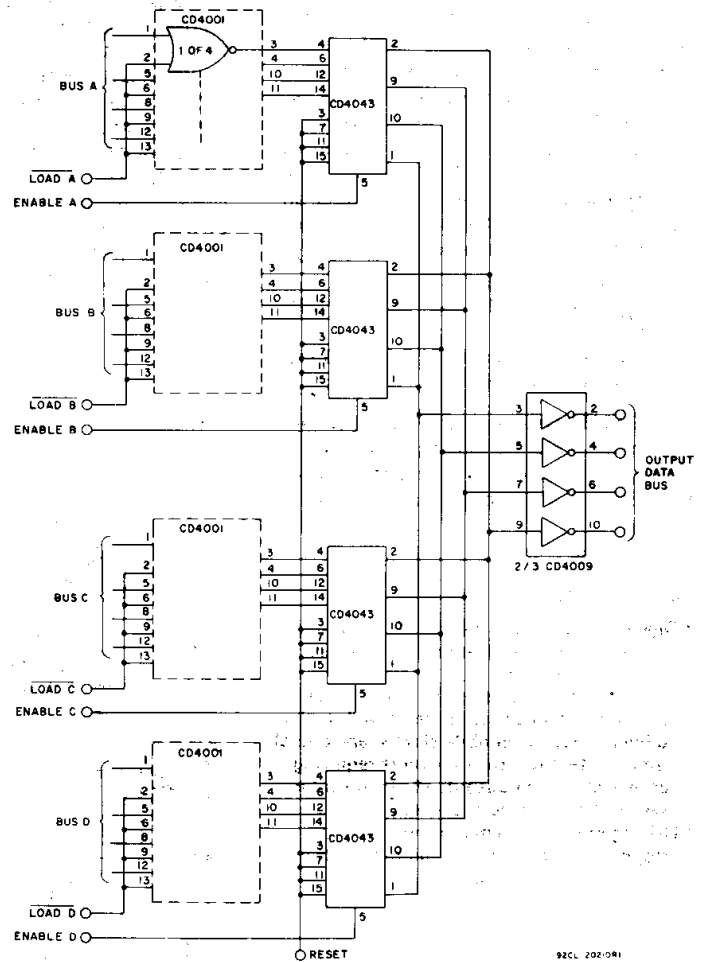


Fig. 13 - ENABLE propagation delay time test circuit and waveforms.

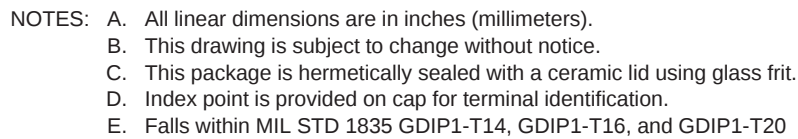
CHIP DIMENSIONS AND PAD LAYOUTS



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

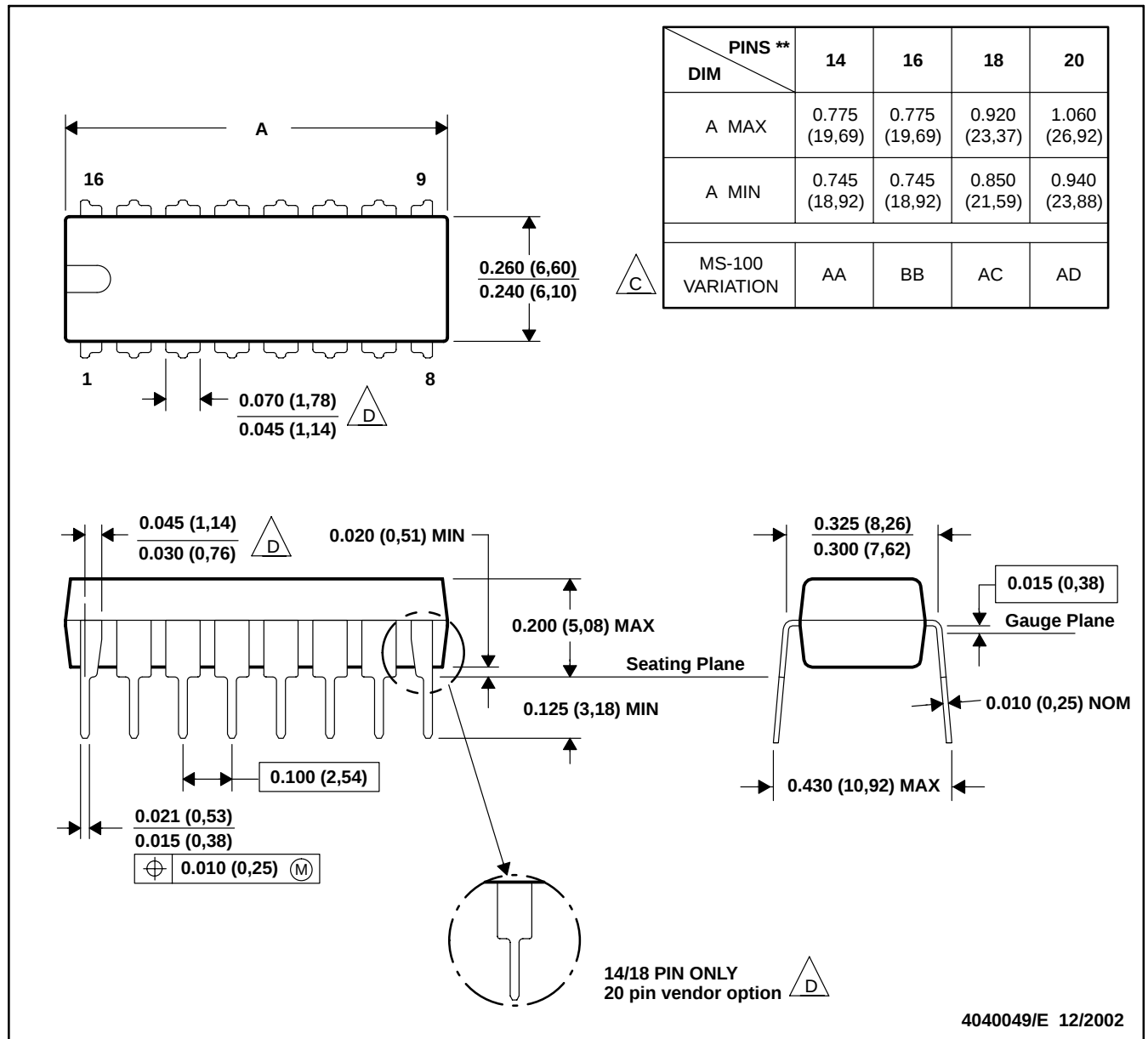


14 LEADS SHOWN

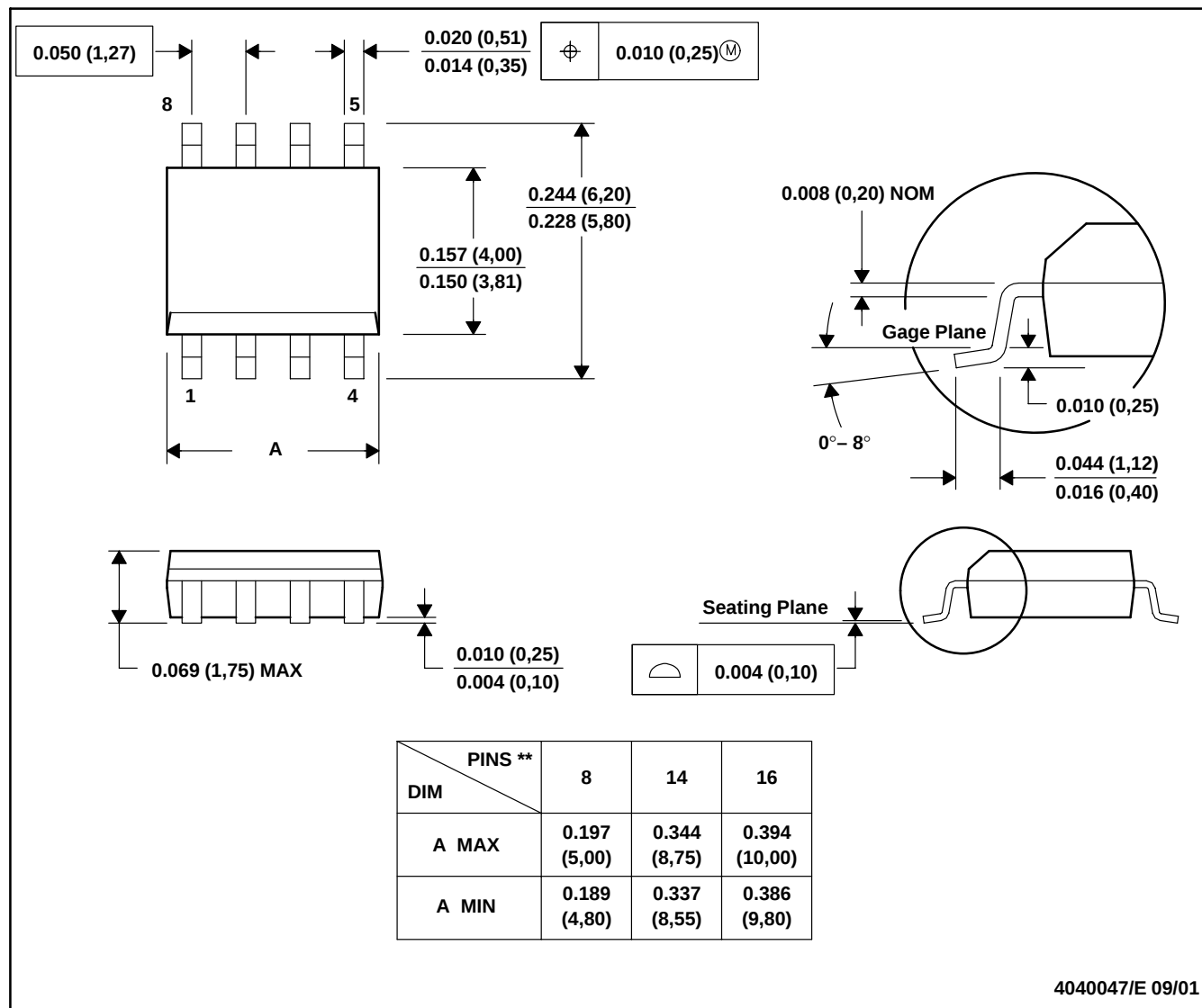


16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

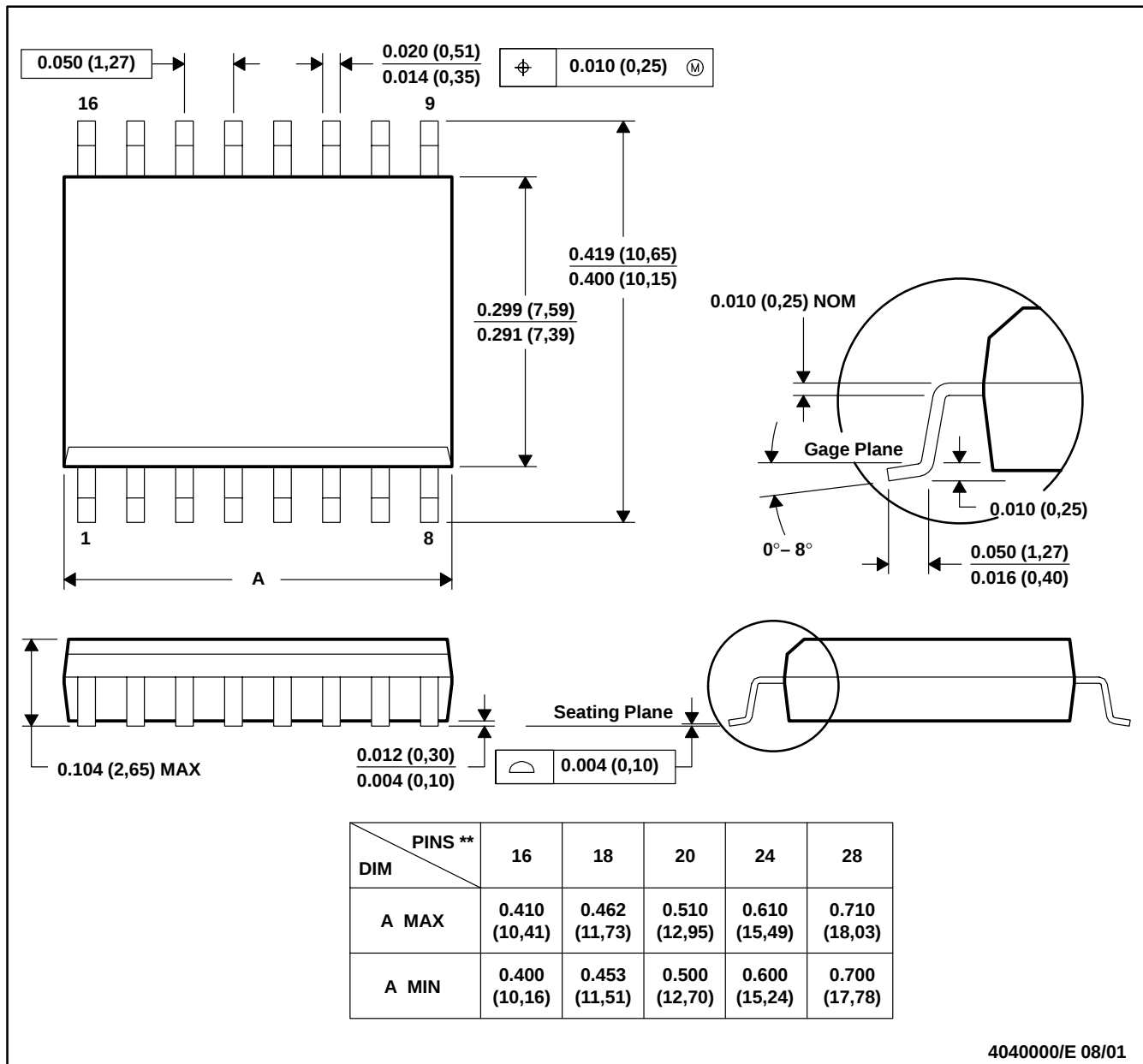
D (R-PDSO-G)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN

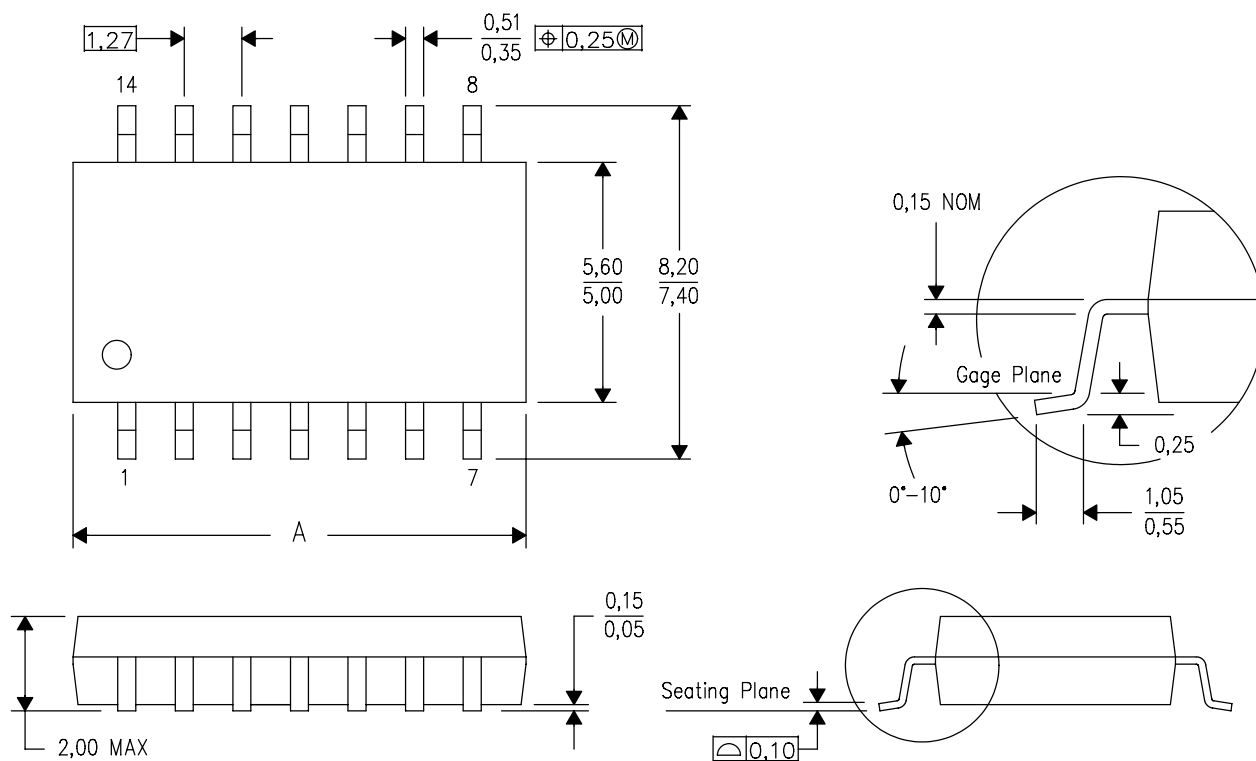


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

NS (R-PDSO-G**)

14-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



PINS **	14	16	20	24
DIM				
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [SAMPLES](#) | [APPLICATION NOTES](#) | [USER GUIDES](#) | [MORE LITERATURE](#)

PRODUCT SUPPORT: [TRAINING](#)

CD4043B, CMOS Quad NOR R/S Latch with 3-State Outputs
DEVICE STATUS: ACTIVE

PARAMETER NAME	CD4043B
Voltage Nodes (V)	5, 10, 15

FEATURES [▲Back to Top](#)

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- Separate SET and RESET inputs for each latch
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- 5-V, 10-V, and 15-V parametric ratings
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 - Holding register in multi-register system
 - Four bits of independent storage with output ENABLE
 - Strobed register
 - General digital logic
 - CD4043B for positive logic systems
 - CD4044B for negative logic systems

Data sheet acquired from Harris Semiconductor

DESCRIPTION [▲Back to Top](#)

CD4043B types are quad cross-coupled 3-state CMOS NOR latches and the CD4044B types are quad cross-coupled 3-state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

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TECHNICAL DOCUMENTS [▲Back to Top](#)

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To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET [▲Back to Top](#)

Full datasheet in Acrobat PDF: [cd4043b.pdf](#) (356 KB,Rev.C) (Updated: 03/12/2003)

APPLICATION NOTES [▲Back to Top](#)

View Application Notes for [Digital Logic](#)

- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics](#) (SCHA004 - Updated: 12/03/2001)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

[▲Back to Top](#)

- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

[▲Back to Top](#)

- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	DSCC NUMBER	PRODUCT CONTENT	SAMPLES
CD4043BDW	SOIC (DW)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4043BE	PDIP (N)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4043BNSR	SOP (NS)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4043BPWR	TSSOP (PW)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION

Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY
CD4043BD	ACTIVE	SOIC (D) 16	-55 TO 125		View Contents	1KU 0.46	40
CD4043BDR	ACTIVE	SOIC (D) 16	-55 TO 125		View Contents	1KU 0.46	2500
CD4043BDW	ACTIVE	SOIC (DW) 16	-55 TO 125		View Contents	1KU 0.24	40
CD4043BDWR	ACTIVE	SOIC (DW) 16	-55 TO 125		View Contents	1KU 0.24	2000

TI INVENTORY STATUS

As Of 08:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY DATE	LEAD TIME
1960*	> 10k 27 May	5 WKS
0*	475 21 Apr	5 WKS
	> 10k 27 May	
0*	6840 30 Apr	6 WKS
	5648 12 May	
0*	4000 30 Apr	6 WKS

REPORTED DISTRIBUTOR INVENTORY

As Of 08:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
None Reported View Distributors		
None Reported View Distributors		
DigiKey Americas	126	BUY NOW
None Reported View Distributors		

									5030 13 May				
									> 10k 03 Jun				
CD4043BE	ACTIVE	PDIP (N) 16	-55 TO 125		View Contents	1KU 0.15	25	0*		5 WKS	EBV Electronik Europe	> 1k	BUY NOW
											Avnet Americas	> 1k	BUY NOW
											DigiKey Americas	> 1k	BUY NOW
											Newark Electronics Americas	> 1k	BUY NOW
											Avnet-SILICA Europe	800	BUY NOW
CD4043BF3A	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 3.02	1	171*	5391 20 May	8 WKS	Avnet Americas	157	BUY NOW
									> 10k 09 Jun		Avnet-SILICA Europe	12	BUY NOW
CD4043BM	OBSOLETE	SOIC (D) 16	-55 TO 125		View Contents	1KU		0*		Call**	None Reported View Distributors		
CD4043BNSR	ACTIVE	SOP (NS) 16	-55 TO 125		View Contents	1KU 0.56	2000	0*	> 10k 30 May	5 WKS	DigiKey Americas	> 1k	BUY NOW
CD4043BPW	ACTIVE	TSSOP (PW) 16	-55 TO 125		View Contents	1KU 0.29	90	0*	> 10k 29 May	5 WKS	None Reported View Distributors		
CD4043BPWR	ACTIVE	TSSOP (PW) 16	-55 TO 125		View Contents	1KU 0.15	2000	0*	2000 16 Apr	5 WKS	DigiKey Americas	> 1k	BUY NOW
									889 21 Apr				
									> 10k 29 May				

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CD4044B, CMOS Quad NAND R/S Latch with 3-State Outputs
DEVICE STATUS: ACTIVE

PARAMETER NAME	CD4044B
Voltage Nodes (V)	5, 10, 15

FEATURES [▲Back to Top](#)

- 3-state outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Applications
 - Holding register in multi-register system
 - Four bits of independent storage with output ENABLE
 - Strobed register
 - General digital logic
 - CD4043B for positive logic systems
 - CD4044B for negative logic systems

Data sheet acquired from Harris Semiconductor

DESCRIPTION [▲Back to Top](#)

CD4043B types are quad cross-coupled 3-state CMOS NOR latches and the CD4044B types are quad cross-coupled 3-state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

The CD4043B and CD4044B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (D, DR, DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

TECHNICAL DOCUMENTS [▲Back to Top](#)

To view the following documents, [Acrobat Reader 4.0](#) is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET [▲Back to Top](#)

Full datasheet in Acrobat PDF: [cd4044b.pdf](#) (356 KB,Rev.C) (Updated: 03/12/2003)

APPLICATION NOTES [▲Back to Top](#)

View Application Notes for [Digital Logic](#)

- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics](#) (SCHA004 - Updated: 12/03/2001)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

[▲Back to Top](#)

- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	DSCC NUMBER	PRODUCT CONTENT	SAMPLES
CD4044BE	PDIP (N)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4044BNSR	SOP (NS)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples

PRICING / AVAILABILITY / PKG

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DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 08:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 08:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
CD4044BD	ACTIVE	SOIC (D) 16	-55 TO 125		View Contents	1KU 0.46	40	2360 *	947 13 May	5 WKS	Avnet Americas	1k	BUY NOW
									> 10k 27 May				
CD4044BDR	ACTIVE	SOIC (D) 16	-55 TO 125		View Contents	1KU 0.46	2500	5000 *	868 21 Apr	5 WKS	Avnet Americas	> 1k	BUY NOW
									947 13 May				
									> 10k 27 May				
CD4044BDW	ACTIVE	SOIC (DW) 16	-55 TO 125		View Contents	1KU 0.26	40	4840 *	> 10k 02 Jun	6 WKS	None Reported View Distributors		
CD4044BDWR	ACTIVE	SOIC (DW) 16	-55 TO 125		View Contents	1KU 0.26	2000	0 *	> 10k 02 Jun	6 WKS	None Reported View Distributors		
CD4044BE	ACTIVE	PDIP (N) 16	-55 TO 125		View Contents	1KU 0.26	25	0 *		5 WKS	Avnet Americas	> 1k	BUY NOW
											EBV Elektronik Europe	> 1k	BUY NOW

												DigiKey Americas	> 1k	BUY NOW
												Newark Electronics Americas	870	BUY NOW
CD4044BF	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 2.49	1	128*	276 06 May	8 WKS		Avnet Americas	79	BUY NOW
									> 10k 20 May					
CD4044BF3A	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 2.90	1	101*	152 06 May	8 WKS		Avnet Americas	110	BUY NOW
									> 10k 20 May			EBV Electronik Europe	2	BUY NOW
CD4044BM	OBSOLETE	SOIC (D) 16	-55 TO 125		View Contents	1KU		0*		Call**		None Reported View Distributors		
CD4044BNSR	ACTIVE	SOP (NS) 16	-55 TO 125		View Contents	1KU 0.56	2000	0*	4267 12 May	5 WKS		DigiKey Americas	> 1k	BUY NOW
									> 10k 30 May					
CD4044BPW	ACTIVE	TSSOP (PW) 16	-55 TO 125		View Contents	1KU 0.29	90	0*	1260 16 Apr	5 WKS		None Reported View Distributors		
									4286 08 May					
									> 10k 29 May					
CD4044BPWR	ACTIVE	TSSOP (PW) 16	-55 TO 125		View Contents	1KU 0.17	2000	0*	4286 08 May	5 WKS		None Reported View Distributors		
									> 10k 29 May					

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