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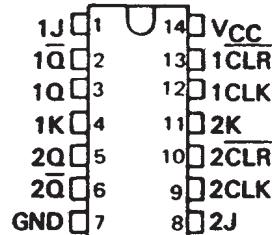
description

The '107 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '107 is a positive pulse-triggered flip-flop. The J-K input data is loaded into the master while the clock is high and transferred to the slave and the outputs on the high-to-low clock transition. For these devices the J and K inputs must be stable while the clock is high.

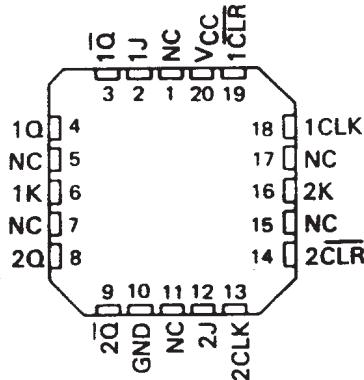
The 'LS107A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \bar{Q} output high.

The SN54107 and the SN54LS107A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74107 and the SN74LS107A are characterized for operation from 0°C to 70°C .

SN54107, SN54LS107A . . . J PACKAGE
SN74107 . . . N PACKAGE
SN74LS107A . . . D OR N PACKAGE
(TOP VIEW)



SN54LS107A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

'107 FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	

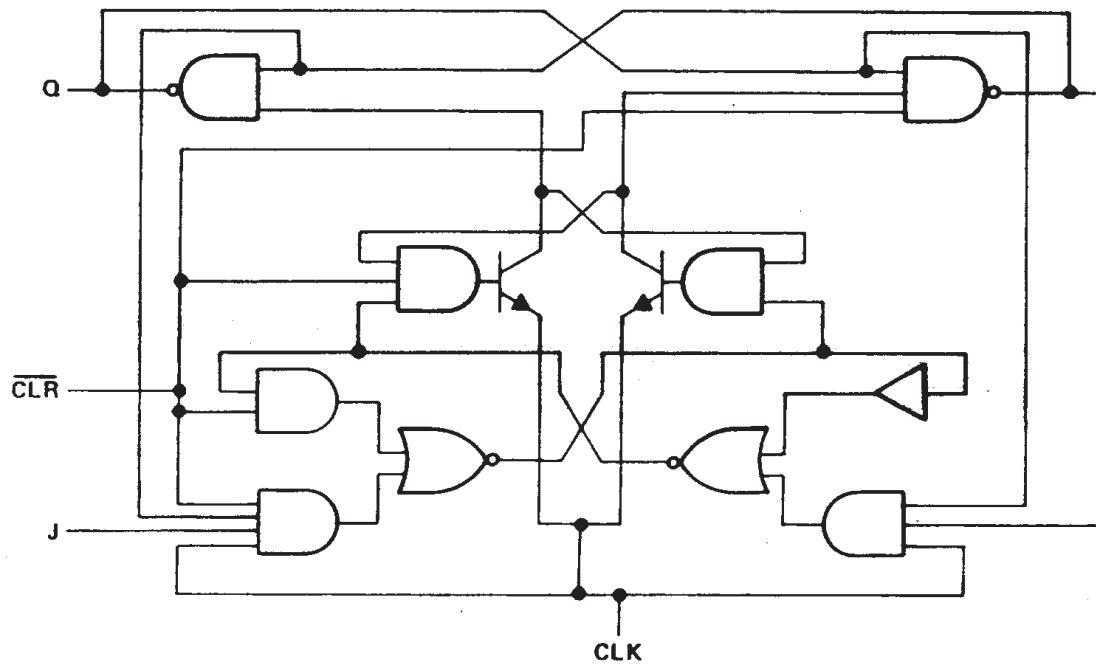
'LS107A FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q_0	\bar{Q}_0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	\bar{Q}_0

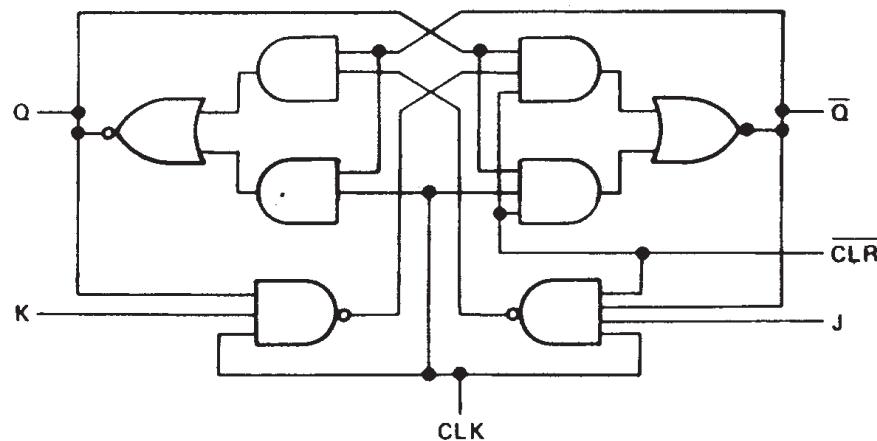
SN54107, SN54LS107A,
SN74107, SN74LS107A
DUAL J-K FLIP-FLOPS WITH CLEAR

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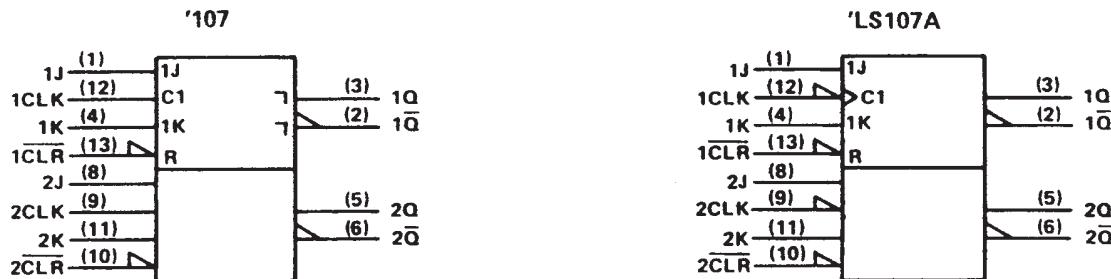
logic diagrams (positive logic)



'LS107A

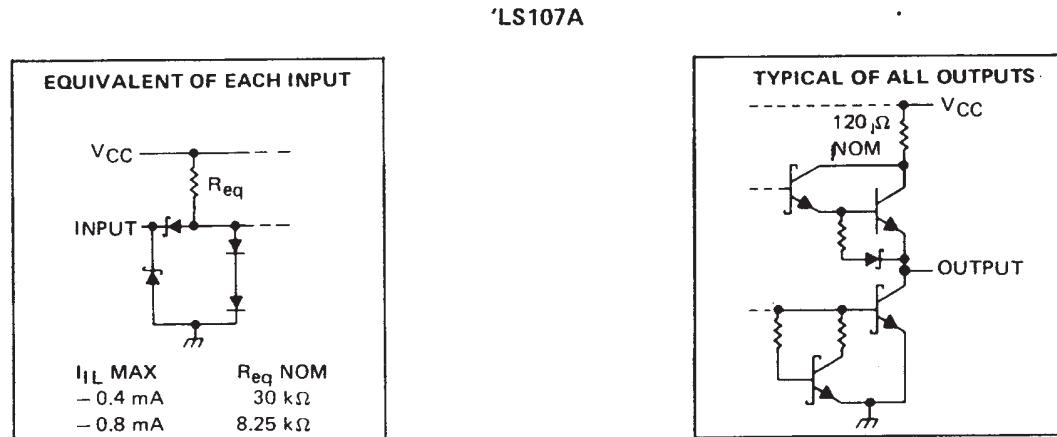
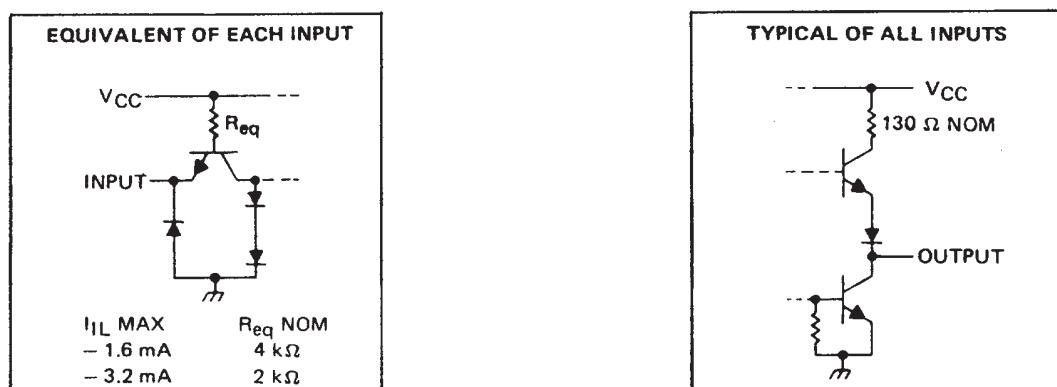


logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: '107	5.5 V
'LS107A	7 V
Operating free-air temperature range: SN54'	- 55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



SN54107, SN74107 DUAL J-K FLIP-FLOPS WITH CLEAR

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recommended operating conditions

			SN54107			SN74107			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current				-0.4			-0.4	mA
I _{OL}	Low-level output current				16			16	mA
t _w	Pulse duration	CLK high	20			20			ns
		CLK low	47			47			
		CLR low	25			25			
t _{su}	Input setup time before CLK1		0			0			ns
t _h	Input hold time-data after CLK1		0			0			ns
T _A	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54107			SN74107			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V _{IK}	V _{CC} = MIN, I _I = -12 mA				-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA	2.4	3.4		2.4	3.4			V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4		V
I _I	V _{CC} = MAX, V _I = 5.5 V				1			1	mA
I _{IH}	J or K All other	V _{CC} = MAX, V _I = 2.4 V	40			40			μA
I _{IL}			80			80			
I _{OS} [§]	V _{CC} = MAX	-20	-57		-18	-57			mA
I _{CC1}	V _{CC} = MAX, See Note 2		10	20		10	20		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time.

[¶]Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 400 Ω, C _L = 15 pF	15	20		MHz
t _{PLH}	CLR	\bar{Q}		16	25		ns
t _{PHL}		Q		25	40		ns
t _{PLH}	CLK	Q or \bar{Q}		16	25		ns
t _{PHL}				25	40		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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SN54LS107A, SN74LS107A
DUAL J-K FLIP-FLOPS WITH CLEAR

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recommended operating conditions

				SN54LS107A			SN74LS107A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
I _{OH}	High-level output current					–0.4			–0.4	mA
I _{OL}	Low-level output current					4			8	mA
f _{clock}	Clock frequency			0		30	0		30	MHz
t _w	Pulse duration	CLK high		20			20			ns
		CLR low		25			25			
t _{su}	Setup time before CLK↓	data high or low		20			20			ns
		CLR inactive		25			25			
t _h	Hold time-data after CLK↓			0			0			ns
T _A	Operating free-air temperature			–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			SN54LS107A			SN74LS107A			UNIT
	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}	V _{CC} = MIN, I _I = –18 mA				–1.5			–1.5		V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = –0.4 mA			2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA				0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA							0.35	0.5	
I _I	J or K				0.1			0.1		mA
	CLR	V _{CC} = MAX, V _I = 7 V			0.3			0.3		
	CLK				0.4			0.4		
I _{IH}	J or K				20			20		μA
	CLR	V _{CC} = MAX, V _I = 2.7 V			60			60		
	CLK				80			80		
I _{IL}	J or K				–0.4			–0.4		mA
	CLR or CLK	V _{CC} = MAX, V _I = 0.4 V			–0.8			–0.8		
I _{OS} [§]	V _{CC} = MAX, See Note 4			–20	–100	–20	–100			mA
I _{CC} (Total)	V _{CC} = MAX, See Note 2			4	6		4	6		mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			MIN	TYP	MAX	UNIT			
f _{max}			R _L = 2 kΩ, C _L = 15 pF			30	45		MHz			
t _{PLH}	CLR or CLK	Q or \bar{Q}				15	20		ns			
t _{PHL}						15	20		ns			

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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