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Jameco Part Number 46130FSC

## MM74HC74A Dual D-Type Flip-Flop with Preset and Clear

### General Description

The MM74HC74A utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and  $\bar{Q}$  outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### Features

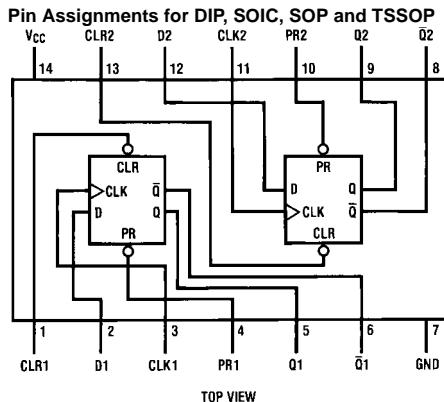
- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40  $\mu$ A maximum (74HC Series)
- Low input current: 1  $\mu$ A maximum
- Fanout of 10 LS-TTL loads

### Ordering Code:

Order Number	Package Number	Package Description
MM74HC74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC74ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



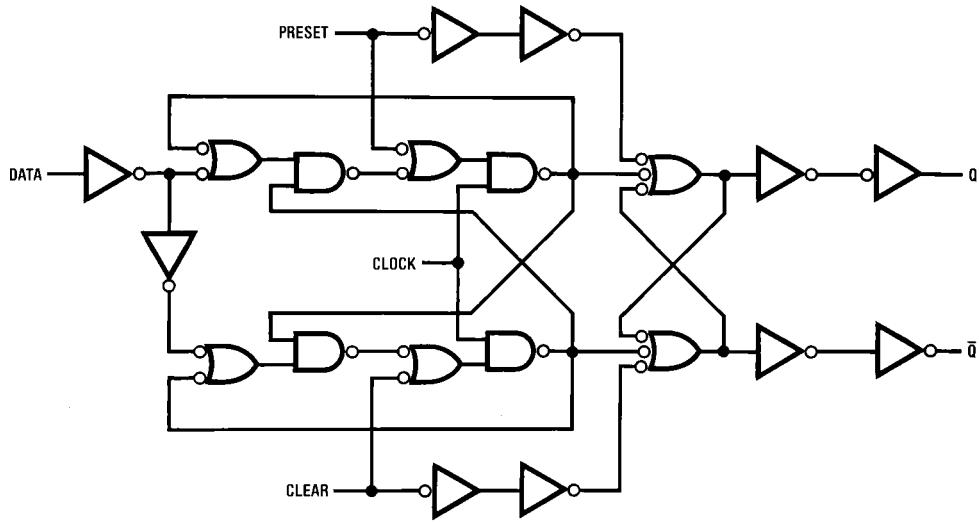
### Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}$ 0

**Note:** Q0 = the level of Q before the indicated input conditions were established.

**Note 1:** This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

## Logic Diagram



Absolute Maximum Ratings (Note 2)				Recommended Operating Conditions					
(Note 3)									
Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V			Supply Voltage ( $V_{CC}$ )	2	6	V		
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC}$ +1.5V			DC Input or Output Voltage	0	$V_{CC}$	V		
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC}$ +0.5V			( $V_{IN}$ , $V_{OUT}$ )					
Clamp Diode Current ( $I_{IK}$ , $I_{OK}$ )	$\pm 20$ mA			Operating Temperature Range ( $T_A$ )	-40	+85	°C		
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA			Input Rise or Fall Times					
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA			( $t_r$ , $t_f$ ) $V_{CC}$ = 2.0V	1000	ns			
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C			$V_{CC}$ = 4.5V	500	ns			
Power Dissipation ( $P_D$ ) (Note 4)	600 mW			$V_{CC}$ = 6.0V	400	ns			
S.O. Package only	500 mW			<b>Note 2:</b> Absolute Maximum Ratings are those values beyond which damage to the device may occur.					
Lead Temperature ( $T_L$ ) (Soldering 10 seconds)	260°C			<b>Note 3:</b> Unless otherwise specified all voltages are referenced to ground.					
				<b>Note 4:</b> Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.					
DC Electrical Characteristics (Note 5)									
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units	
				Typ		Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15	V	
			6.0V		4.2	4.2	4.2	V	
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35	V	
			6.0V		1.8	1.8	1.8	V	
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	5.9	V	
			$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V	4.3	3.98	3.84	3.7	V
				6.0V	5.2	5.48	5.34	5.2	V
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1	V	
			6.0V	0	0.1	0.1	0.1	V	
			$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
				6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		4.0	40	80	$\mu A$	
<b>Note 5:</b> For a power supply of $5V \pm 10\%$ the worst case output voltages ( $V_{OH}$ , and $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ , $I_{CC}$ , and $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.									

## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		72	30	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Clock to Q or $\bar{Q}$		10	30	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Preset or Clear to Q or $\bar{Q}$		17	40	ns
$t_{REM}$	Minimum Removal Time, Preset or Clear to Clock		6	5	ns
$t_s$	Minimum Setup Time Data to Clock		10	20	ns
$t_H$	Minimum Hold Time Clock to Data		0	0	ns
$t_W$	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

## AC Electrical Characteristics

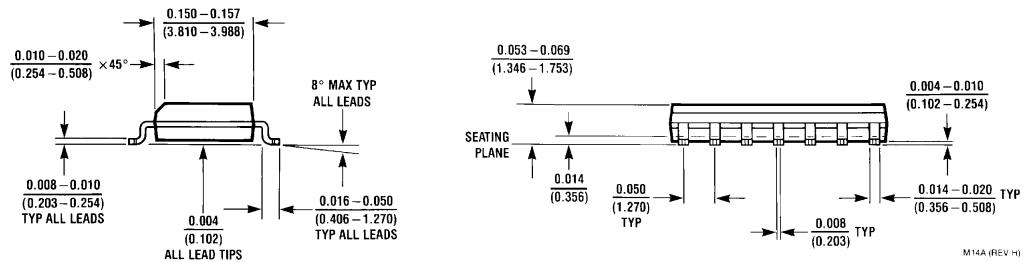
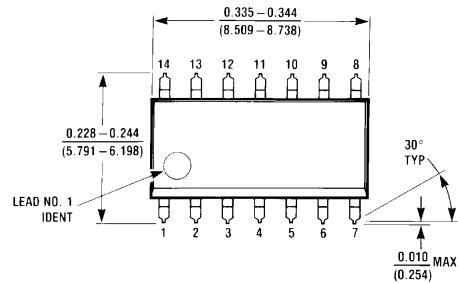
$C_L = 50 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		Guaranteed Limits	Units
				Typ			
$f_{MAX}$	Maximum Operating Frequency		2.0V	22	6	5	4
			4.5V	72	30	24	20
			6.0V	94	35	28	24
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Clock to Q or $\bar{Q}$		2.0V	34	110	140	165
			4.5V	12	22	28	33
			6.0V	10	19	24	28
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Preset or Clear To Q or $\bar{Q}$		2.0V	66	150	190	225
			4.5V	20	30	38	45
			6.0V	16	26	33	38
$t_{REM}$	Minimum Removal Time Preset or Clear To Clock		2.0V	20	50	65	75
			4.5V	6	10	13	15
			6.0V	5	9	11	13
$t_s$	Minimum Setup Time Data to Clock		2.0V	35	80	100	120
			4.5V	10	16	20	24
			6.0V	8	14	17	20
$t_H$	Minimum Hold Time Clock to Data		2.0V		0	0	0
			4.5V		0	0	0
			6.0V		0	0	0
$t_W$	Minimum, Pulse Width Clock, Preset or Clear		2.0V	30	80	101	119
			4.5V	9	16	20	24
			6.0V	8	14	17	20
$t_{TLH}, t_{THL}$	Maximum Output Rise and Fall Time		2.0V	25	75	95	110
			4.5V	7	15	19	22
			6.0V	6	13	16	19
$t_r, t_f$	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000
			4.5V		500	500	500
			6.0V		400	400	400
$C_{PD}$	Power Dissipation Capacitance (Note 6)	(per flip-flop)		80			pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	pF

**Note 6:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

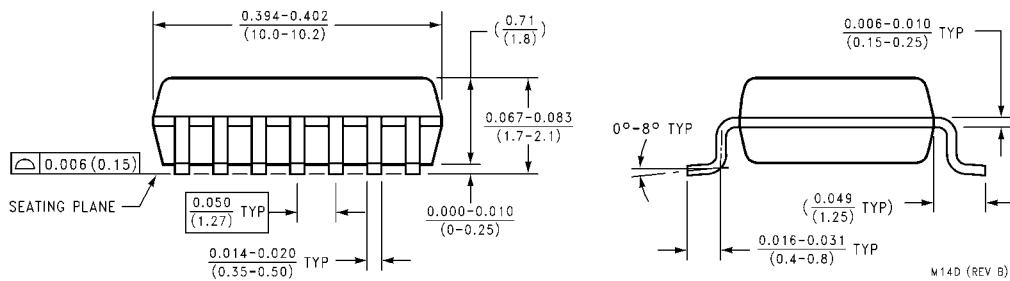
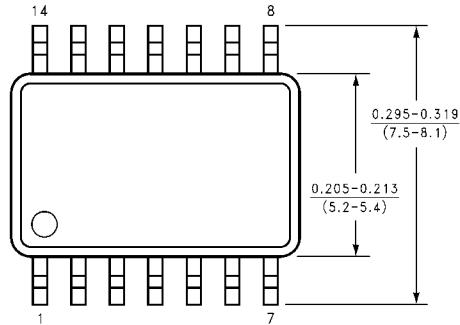
### Physical Dimensions

inches (millimeters) unless otherwise noted



M14A (REV. H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow  
Package Number M14A

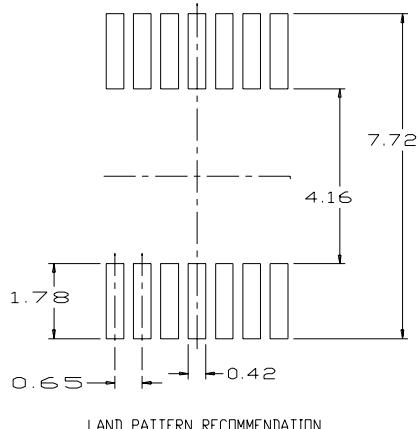
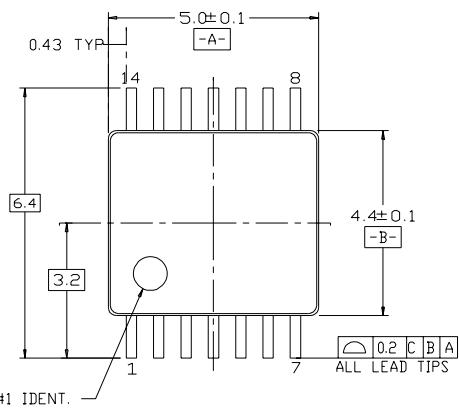


M14D (REV. B)

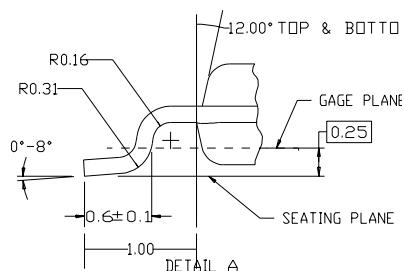
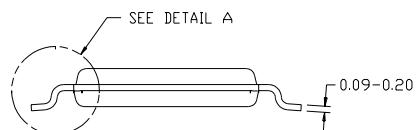
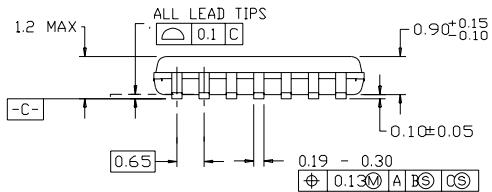
14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE



LAND PATTERN RECOMMENDATION

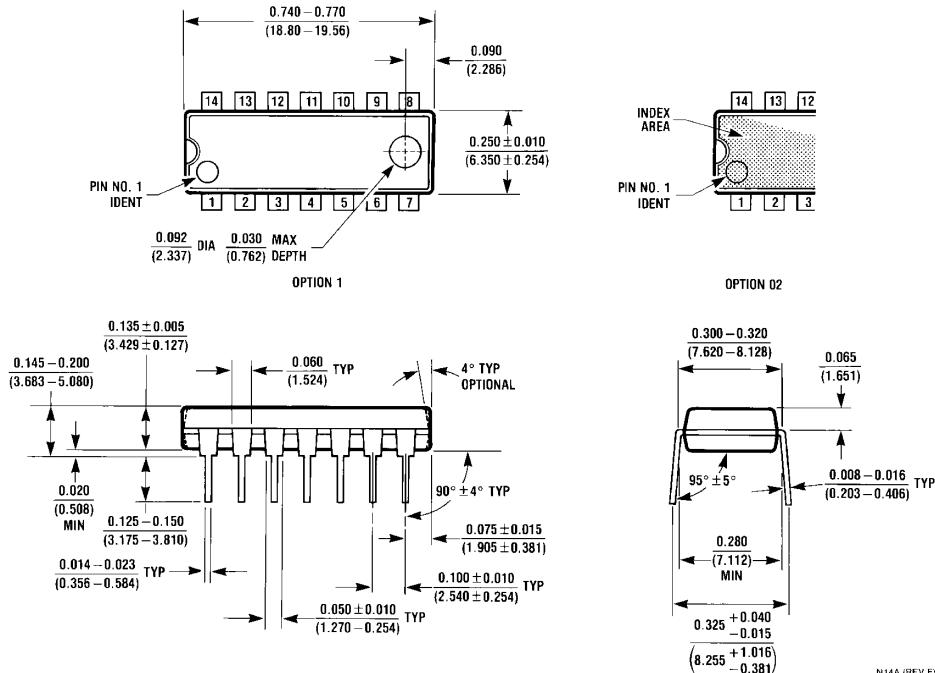


### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC14

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N14A

N14A (REV F)

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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