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# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT4017

### Johnson decade counter with 10 decoded outputs

Product specification  
File under Integrated Circuits, IC06

December 1990

## Johnson decade counter with 10 decoded outputs

## 74HC/HCT4017

## FEATURES

- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs ( $Q_0$  to  $Q_9$ ), an active LOW output from the most significant flip-flop ( $\bar{Q}_{5-9}$ ), active HIGH and active LOW clock inputs ( $CP_0$  and

$CP_1$ ) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at  $CP_0$  while  $CP_1$  is LOW or a HIGH-to-LOW transition at  $CP_1$  while  $CP_0$  is HIGH (see also function table).

When cascading counters, the  $\bar{Q}_{5-9}$  output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the  $CP_0$  input of the next counter.

A HIGH on MR resets the counter to zero ( $Q_0 = \bar{Q}_{5-9} = \text{HIGH}$ ;  $Q_1$  to  $Q_9 = \text{LOW}$ ) independent of the clock inputs ( $CP_0$  and  $CP_1$ ).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

## QUICK REFERENCE DATA

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $CP_0, \bar{CP}_1$ to $Q_n$	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	20	21	ns
$f_{max}$	maximum clock frequency		77	67	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	35	36	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$

For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	$Q_0$ to $Q_9$	decoded outputs
8	GND	ground (0 V)
12	$\bar{Q}_{5-9}$	carry output (active LOW)
13	$\bar{CP}_1$	clock input (HIGH-to-LOW, edge-triggered)
14	$CP_0$	clock input (LOW-to-HIGH, edge-triggered)
15	MR	master reset input (active HIGH)
16	$V_{CC}$	positive supply voltage

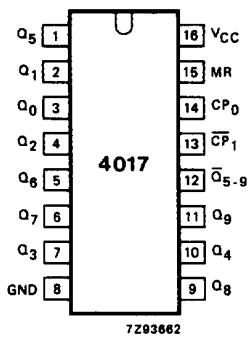


Fig.1 Pin configuration.

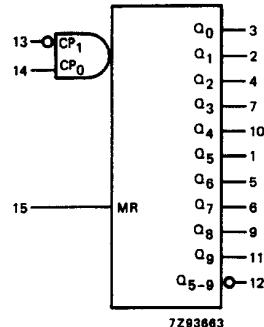


Fig.2 Logic symbol.

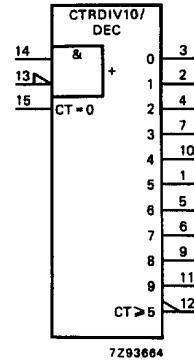


Fig.3 IEC logic symbol.

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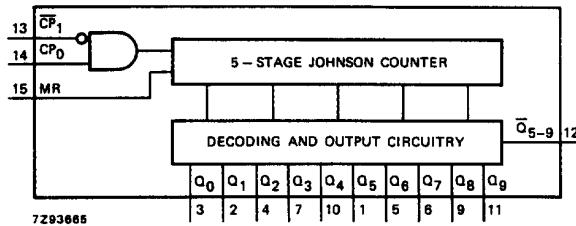


Fig.4 Functional diagram.

## FUNCTION TABLE

MR	CP <sub>0</sub>	CP <sub>1</sub>	OPERATION
H	X	X	Q <sub>0</sub> = Q <sub>5-9</sub> = H; Q <sub>1</sub> to Q <sub>9</sub> = L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

## Notes

1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- ↑ = LOW-to-HIGH clock transition
- ↓ = HIGH-to-LOW clock transition

# Johnson decade counter with 10 decoded outputs

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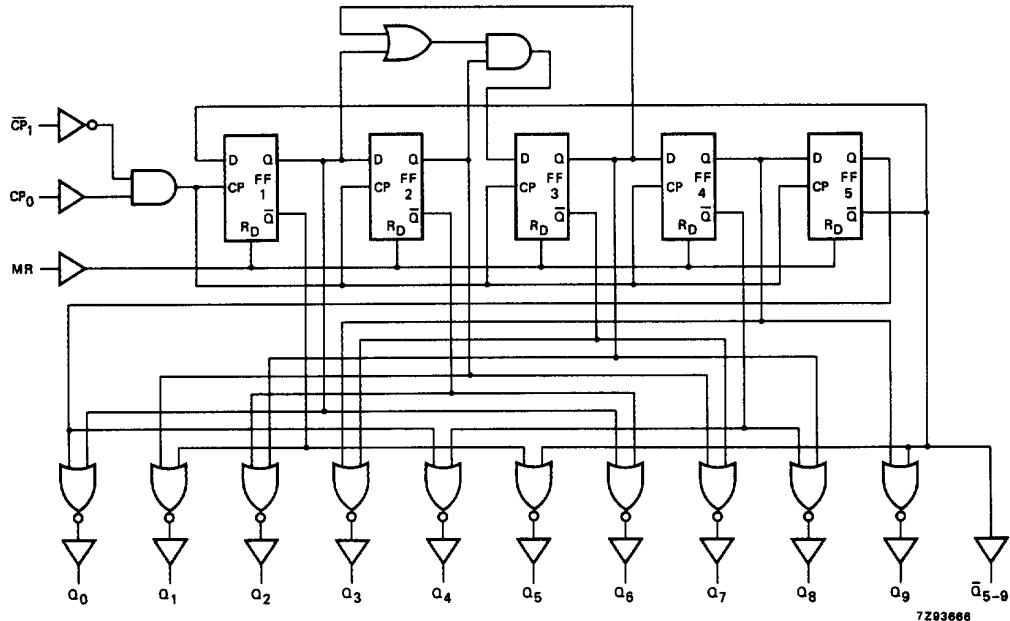


Fig.5 Logic diagram.

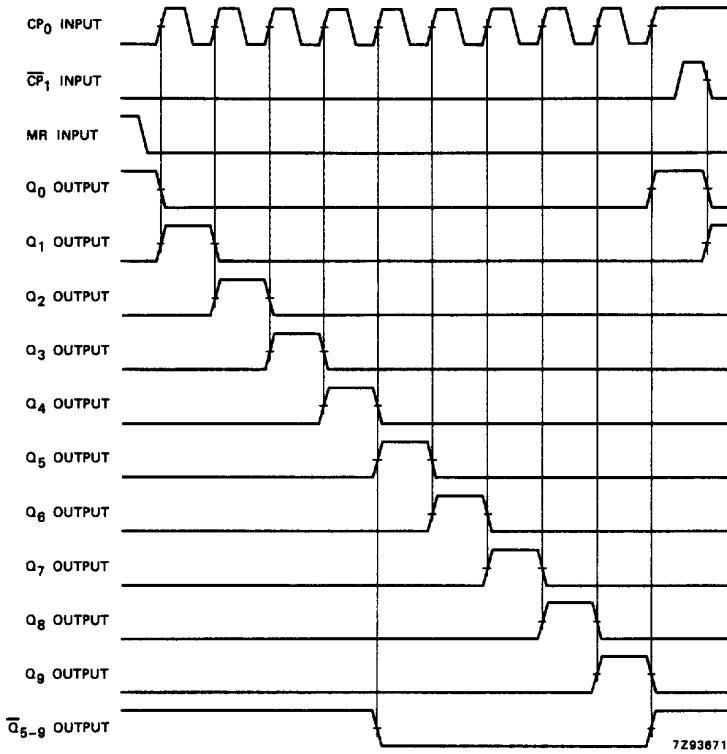


Fig.6 Timing diagram.

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**DC CHARACTERISTICS FOR 74HC**For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I<sub>CC</sub> category: MSI

## Johnson decade counter with 10 decoded outputs

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## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	WAVEFORMS		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>0</sub> to Q <sub>n</sub>	63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.9		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>0</sub> to Q̄ <sub>5-9</sub>	63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.9		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP̄ <sub>1</sub> to Q <sub>n</sub>	61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP̄ <sub>1</sub> to Q̄ <sub>5-9</sub>	61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.9		
t <sub>PHL</sub>	propagation delay MR to Q <sub>1-9</sub>	52 19 15	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.8		
t <sub>PLH</sub>	propagation delay MR to Q̄ <sub>5-9</sub> , Q <sub>0</sub>	55 20 16	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.8		
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.9		
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.8		
t <sub>W</sub>	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.8		
t <sub>rem</sub>	removal time MR to CP <sub>0</sub> , CP̄ <sub>1</sub>	5 5 5	-17 -6 -5		5 5 5		5 5 5	ns	2.0 4.5 6.0	Fig.8		
t <sub>su</sub>	set-up time CP̄ <sub>1</sub> to CP <sub>0</sub> ; CP <sub>0</sub> to CP̄ <sub>1</sub>	50 10 9	-8 -3 -2		65 13 11		75 15 13	ns	2.0 4.5 6.0	Fig.7		
t <sub>h</sub>	hold time CP <sub>0</sub> to CP̄ <sub>1</sub> ; CP <sub>1</sub> to CP <sub>0</sub>	50 10 9	17 6 5		65 13 11		75 15 13	ns	2.0 4.5 6.0	Fig.7		
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 25	23 70 83		4.8 24 28		4.0 20 24	MHz	2.0 4.5 6.0	Fig.8		

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**DC CHARACTERISTICS FOR 74HCT**For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I<sub>CC</sub> category: MSI**Note to HCT types**The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP <sub>1</sub>	0.40
CP <sub>0</sub>	0.25
MR	0.50

## Johnson decade counter with 10 decoded outputs

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## AC CHARACTERISTICS FOR 74HCT

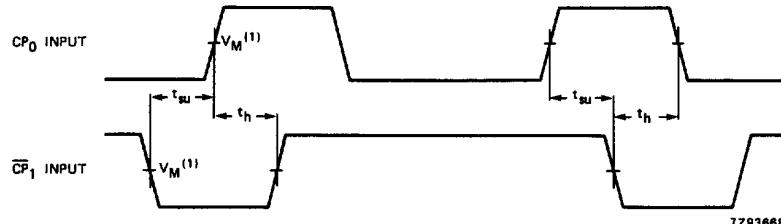
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $CP_0$ to $Q_n$	25	46		58		69	ns	4.5	Fig.9		
$t_{PHL}/t_{PLH}$	propagation delay $CP_0$ to $Q_{5-9}$	25	46		58		69	ns	4.5	Fig.9		
$t_{PHL}/t_{PLH}$	propagation delay $CP_1$ to $Q_n$	25	50		63		75	ns	4.5	Fig.9		
$t_{PHL}/t_{PLH}$	propagation delay $CP_1$ to $Q_{5-9}$	25	50		63		75	ns	4.5	Fig.9		
$t_{PHL}$	propagation delay MR to $Q_{1-9}$	22	46		58		69	ns	4.5	Fig.8		
$t_{PLH}$	propagation delay MR to $Q_{5-9}, Q_0$	20	46		58		69	ns	4.5	Fig.8		
$t_{THL}/t_{TLH}$	output transition time	7	15		19		22	ns	4.5	Fig.9		
$t_W$	clock pulse width HIGH or LOW	16	7		20		24	ns	4.5	Fig.8		
$t_W$	master reset pulse width; HIGH	16	4		20		24	ns	4.5	Fig.8		
$t_{rem}$	removal time MR to $CP_0, \overline{CP_1}$	5	-5		5		5	ns	4.5	Fig.8		
$t_{su}$	set-up time $\overline{CP_1}$ to $CP_0$ ; $CP_0$ to $\overline{CP_1}$	10	-3		13		15	ns	4.5	Fig.7		
$t_h$	hold time $CP_0$ to $\overline{CP_1}$ ; $\overline{CP_1}$ to $CP_0$	10	6		13		15	ns	4.5	Fig.7		
$f_{max}$	maximum clock pulse frequency	30	61		24		20	ns	4.5	Fig.8		

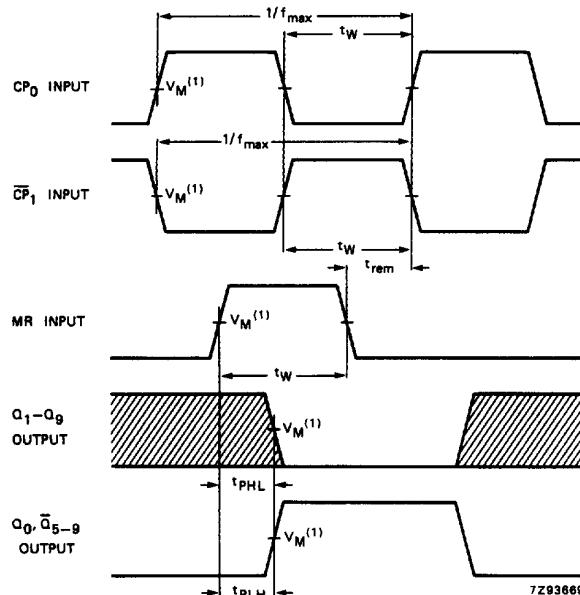
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## AC WAVEFORMS



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the hold and set-up times for  $CP_0$  to  $\overline{CP}_1$  and  $\overline{CP}_1$  to  $CP_0$ .

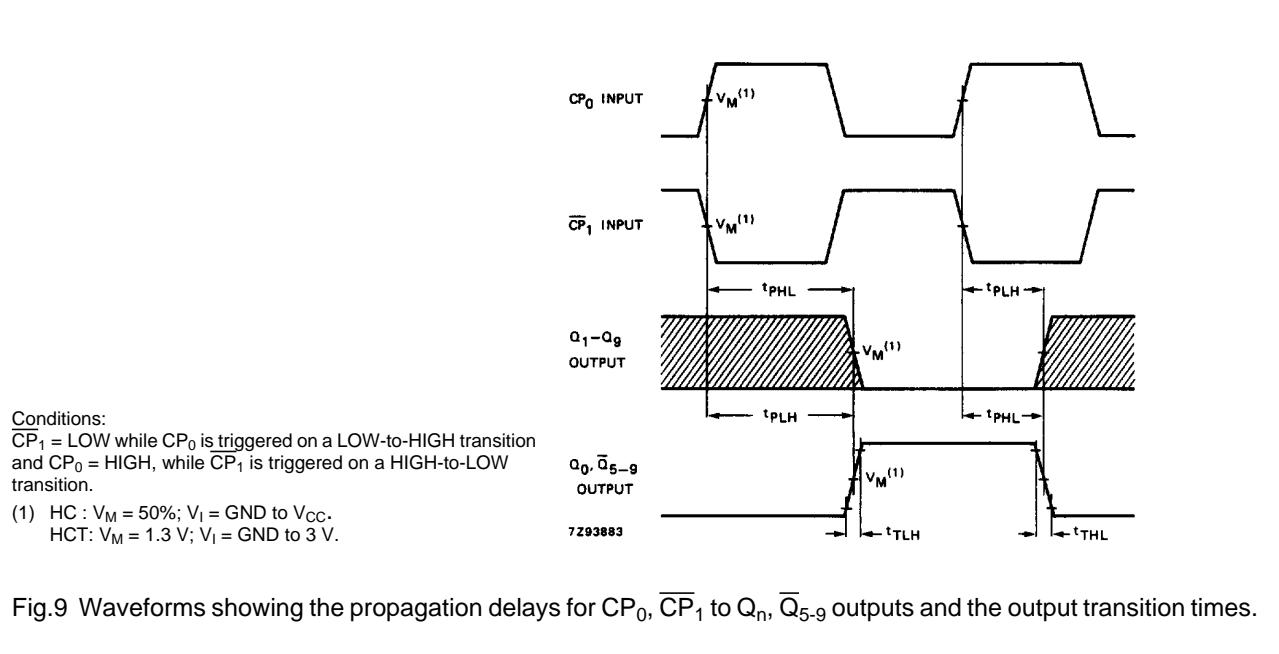
Conditions:  
 $CP_1 = \text{LOW}$  while  $CP_0$  is triggered on a LOW-to-HIGH transition and  $CP_0 = \text{HIGH}$ , while  $CP_1$  is triggered on a HIGH-to-LOW transition.

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.8 Waveforms showing the minimum pulse widths for  $CP_0$ ,  $\overline{CP}_1$  and MR inputs; the recovery time for MR and the propagation delays for MR to  $Q_n$  and  $\overline{Q}_{5-9}$  outputs.

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Fig.9 Waveforms showing the propagation delays for  $CP_0$ ,  $\overline{CP_1}$  to  $Q_n$ ,  $\overline{Q}_{5-9}$  outputs and the output transition times.

## Johnson decade counter with 10 decoded outputs

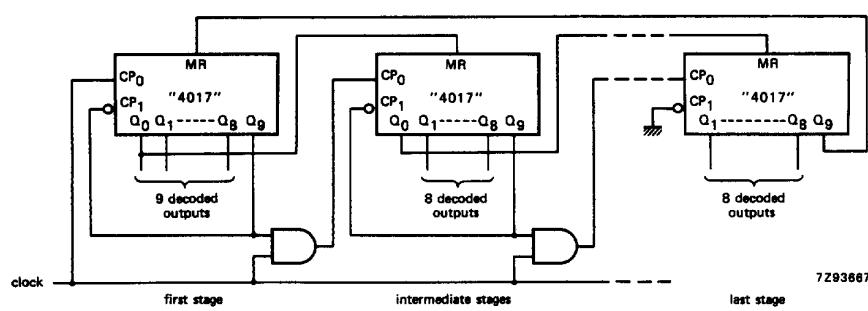
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## APPLICATION INFORMATION

Some applications for the "4017" are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 10 shows a technique for extending the number of decoded output states for the "4017". Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



It is essential not to enable the counter on  $\overline{CP_1}$  when  $CP_0$  is HIGH, or on  $CP_0$  when  $\overline{CP_1}$  is LOW, as this would cause an extra count.

Fig.10 Counter expansion

Figure 11 shows an example of a divide-by 2 through divide-by 10 circuit using one "4017". Since "4017" has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting a RC network at the MR input.

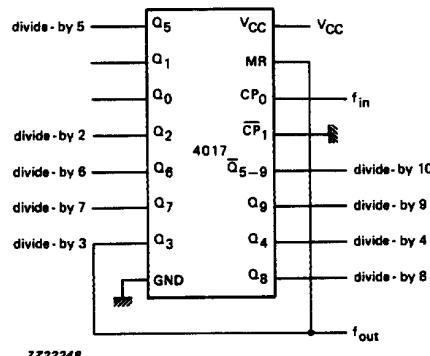


Fig.11 Divide-by 2 through divide-by 10.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".