

Distributed by:



**[www.Jameco.com](http://www.Jameco.com) ♦ 1-800-831-4242**

The content and copyrights of the attached  
material are the property of its owner.

Jameco Part Number 45073FSC

## MM74HCT373 • MM74HCT374

### 3-STATE Octal D-Type Latch •

### 3-STATE Octal D-Type Flip-Flop

#### General Description

The MM74HCT373 octal D-type latches and MM74HCT374 Octal D-type flip flops advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The 3-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to  $V_{CC}$  and ground.

When the MM74HCT373 LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time

requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

#### Features

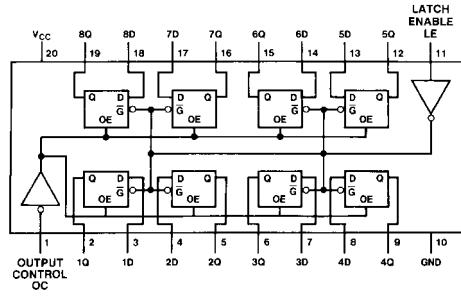
- TTL input characteristic compatible
- Typical propagation delay: 20 ns
- Low input current: 1  $\mu$ A maximum
- Low quiescent current: 80  $\mu$ A maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

#### Ordering Code:

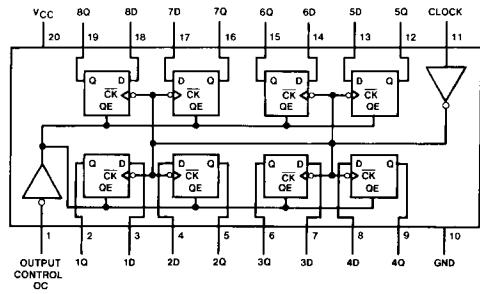
Order Number	Package Number	Package Descriptions
MM74HCT373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HCT374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagrams



Top View  
MM74HCT373



Top View  
MM74HCT374

### Truth Tables

MM74HCT373

Output Control	LE	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

H = HIGH Level

L = LOW Level

$Q_0$  = Level of output before steady-state input conditions were established.

Z = High Impedance

MM74HCT374

Output Control	Clock	Data	Output (374)
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

H = HIGH Level

L = LOW Level

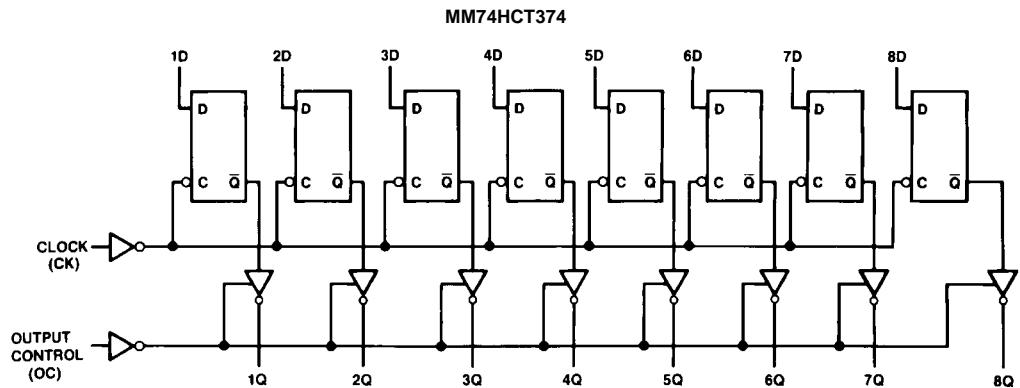
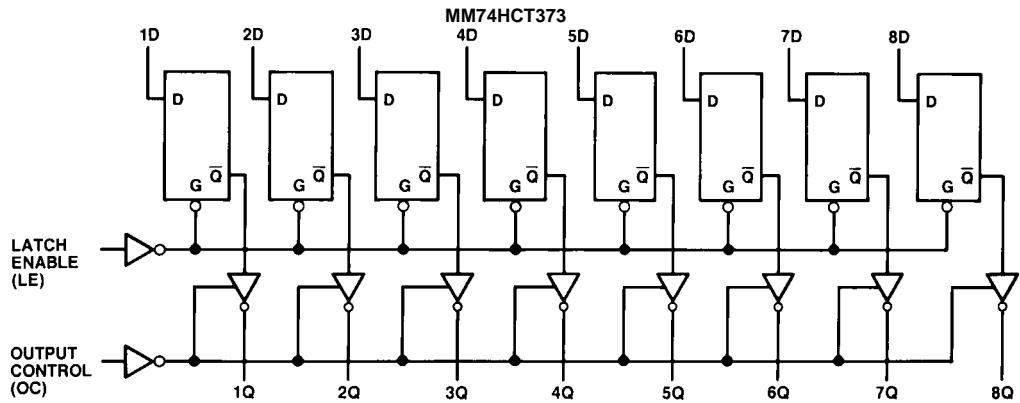
X = Don't Care

↑ = Transition from LOW-to-HIGH

Z = High Impedance State

$Q_0$  = The level of the output before steady state input conditions were established.

**Logic Diagrams**



Absolute Maximum Ratings <sup>(Note 1)</sup>			Recommended Operating Conditions			
(Note 2)						
Supply Voltage ( $V_{CC}$ )	–0.5 to +7.0V		Min	Max	Units	
DC Input Voltage ( $V_{IN}$ )	–1.5 to $V_{CC}$ +1.5V		Supply Voltage ( $V_{CC}$ )	4.5	5.5	V
DC Output Voltage ( $V_{OUT}$ )	–0.5 to $V_{CC}$ +0.5V		DC Input or Output Voltage ( $V_{IN}$ , $V_{OUT}$ )	0	$V_{CC}$	V
Clamp Diode Current ( $I_{IK}$ , $I_{OK}$ )	±20 mA		Operating Temperature Range ( $T_A$ )	–40	+85	°C
DC Output Current, per pin ( $I_{OUT}$ )	±35 mA		Input Rise or Fall Times ( $t_r$ , $t_f$ )		500	ns
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±70 mA					
Storage Temperature Range ( $T_{STG}$ )	–65°C to +150°C					
Power Dissipation ( $P_D$ ) (Note 3)	600 mW					
S.O. Package only	500 mW					
Lead Temperature ( $T_L$ ) (Soldering 10 seconds)	260°C					
<b>DC Electrical Characteristics</b>						
$V_{CC} = 5V \pm 10\%$ (unless otherwise specified)						
Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$	$T_A = -40 \text{ to } 85^\circ\text{C}$	$T_A = -55 \text{ to } 125^\circ\text{C}$	Units
			Typ	Guaranteed Limits		
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0	2.0	2.0	V
$V_{IL}$	Maximum LOW Level Input Voltage		0.8	0.8	0.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu\text{A}$ $ I_{OUT}  = 6.0 \text{ mA}$ , $V_{CC} = 4.5\text{V}$ $ I_{OUT}  = 7.2 \text{ mA}$ , $V_{CC} = 5.5\text{V}$	$V_{CC}$ 4.2 5.7	$V_{CC} - 0.1$ 3.98 4.98	$V_{CC} - 0.1$ 3.84 4.84	$V_{CC} - 0.1$ 3.7 4.7
$V_{OL}$	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 20 \mu\text{A}$ $ I_{OUT}  = 6.0 \text{ mA}$ , $V_{CC} = 4.5\text{V}$ $ I_{OUT}  = 7.2 \text{ mA}$ , $V_{CC} = 5.5\text{V}$	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	$V$ V V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, $V_{IH}$ or $V_{IL}$		±0.1	±1.0	±1.0
$I_{OZ}$	Maximum 3-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Enable = $V_{IH}$ or $V_{IL}$		±0.5	±5.0	±10
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$ $V_{IN} = 2.4\text{V}$ or $0.5\text{V}$ (Note 4)		8.0 1.0	80 1.3	160 1.5

**Note 4:** Measured per pin. All others tied to  $V_{CC}$  or ground.

### AC Electrical Characteristics

MM74HCT373:  $V_{CC} = 5.0V$ ,  $t_r = t_f = 6$  ns  $T_A = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Data to Output	$C_L = 45$ pF	18	25	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Latch Enable to Output	$C_L = 45$ pF	21	30	ns
$t_{PZH}, t_{PZL}$	Maximum Enable Propagation Delay Control to Output	$C_L = 45$ pF $R_L = 1$ k $\Omega$	20	28	ns
$t_{PHZ}, t_{PLZ}$	Maximum Disable Propagation Delay Control to Output	$C_L = 5$ pF $R_L = 1$ k $\Omega$	18	25	ns
$t_W$	Minimum Clock Pulse Width			16	ns
$t_S$	Minimum Setup Time Data to Clock			5	ns
$t_H$	Minimum Hold Time Clock to Data			10	ns

### AC Electrical Characteristics

MM74HCT373:  $V_{CC} = 5.0V \pm 10\%$ ,  $t_r = t_f = 6$  ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
			Typ	Guaranteed Limits			
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Data to Output	$C_L = 50$ pF $C_L = 150$ pF	22 30	30 40	37 50	45 60	ns ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Latch Enable to Output	$C_L = 50$ pF $C_L = 150$ pF	25 32	35 45	44 56	53 68	ns ns
$t_{PZH}, t_{PZL}$	Maximum Enable Propagation Delay Control to Output	$C_L = 50$ pF $C_L = 150$ pF $R_L = 1$ k $\Omega$	21 30	30 40	37 50	45 60	ns ns
$t_{PHZ}, t_{PLZ}$	Maximum Disable Propagation Delay Control to Output	$C_L = 50$ pF $R_L = 1$ k $\Omega$	21	30	37	45	ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time	$C_L = 50$ pF	8	12	15	18	ns
$t_W$	Minimum Clock Pulse Width			16	20	24	ns
$t_S$	Minimum Setup Time Data to Clock			5	6	8	ns
$t_H$	Minimum Hold Time Clock to Data			10	13	20	ns
$C_{IN}$	Maximum Input Capacitance			10	10	10	pF
$C_{OUT}$	Maximum Output Capacitance			20	20	20	pF
$C_{PD}$	Power Dissipation Capacitance (Note 5)	$OC = V_{CC}$ $OC = GND$		5 52			pF pF

Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

### AC Electrical Characteristics

MM74HCT374:  $V_{CC} = 5.0V$ ,  $t_r = t_f = 6\text{ ns}$   $T_A = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Clock Frequency		50	30	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay to Output	$C_L = 45\text{ pF}$	20	32	ns
$t_{PZH}, t_{PZL}$	Maximum Enable Propagation Delay Control to Output	$C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$	19	28	ns
$t_{PHZ}, t_{PLZ}$	Maximum Disable Propagation Delay Control to Output	$C_L = 5\text{ pF}$ $R_L = 1\text{ k}\Omega$	17	25	ns
$t_W$	Minimum Clock Pulse Width			20	ns
$t_S$	Minimum Setup Time Data to Clock			5	ns
$t_H$	Minimum Hold Time Clock to Data			16	ns

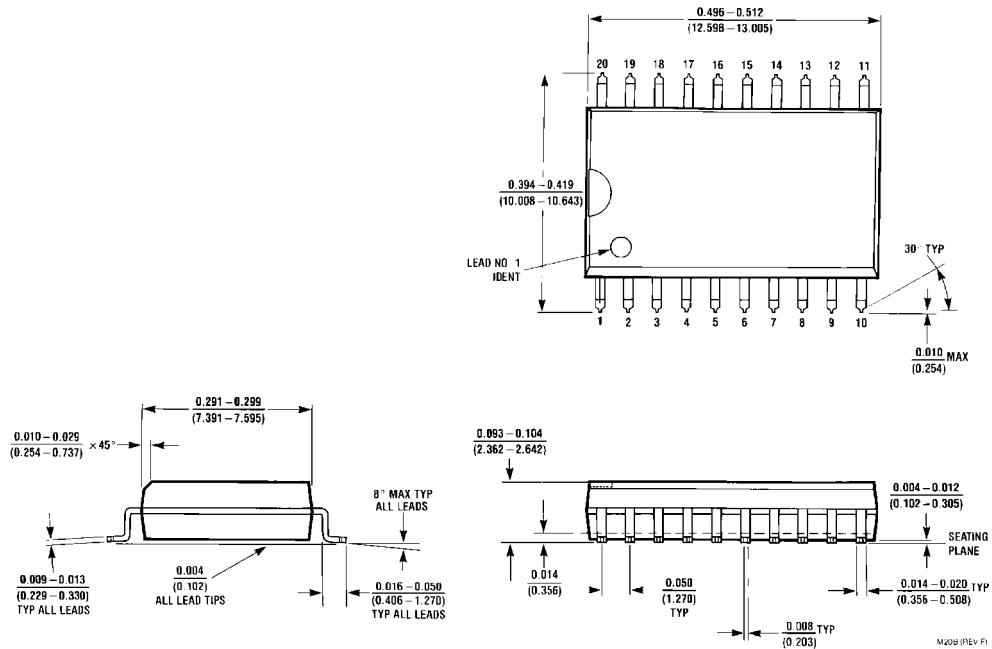
### AC Electrical Characteristics

MM74HCT374:  $V_{CC} = 5.0V \pm 10\%$ ,  $t_r = t_f = 6\text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		Guaranteed Limits	Units
			Typ			
$f_{MAX}$	Maximum Clock Frequency		30	24	20	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay to Output	$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	22 30	36 46	45 57	ns ns
$t_{PZH}, t_{PZL}$	Maximum Enable Propagation Delay Control to Output	$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ $R_L = 1\text{ k}\Omega$	21 30	30 40	37 50	45 60
$t_{PHZ}, t_{PLZ}$	Maximum Disable Propagation Delay Control to Output	$C_L = 50\text{ pF}$ $R_L = 1\text{ k}\Omega$	21	30	37	45
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time	$C_L = 50\text{ pF}$	8	12	15	ns
$t_W$	Minimum Clock Pulse Width			16	20	ns
$t_S$	Minimum Setup Time Data to Clock			20	25	ns
$t_H$	Minimum Hold Time Clock to Data			5	5	ns
$C_{IN}$	Maximum Input Capacitance			10	10	pF
$C_{OUT}$	Maximum Output Capacitance			20	20	pF
$C_{PD}$	Power Dissipation Capacitance (Note 6)	$OC = V_{CC}$ $OC = GND$		5 58		pF pF

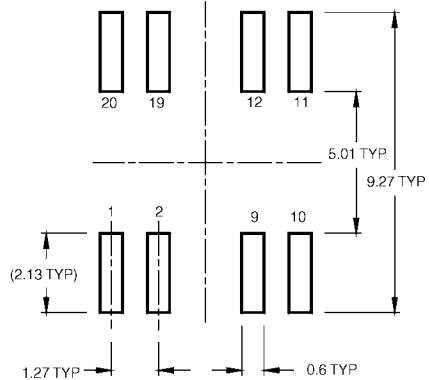
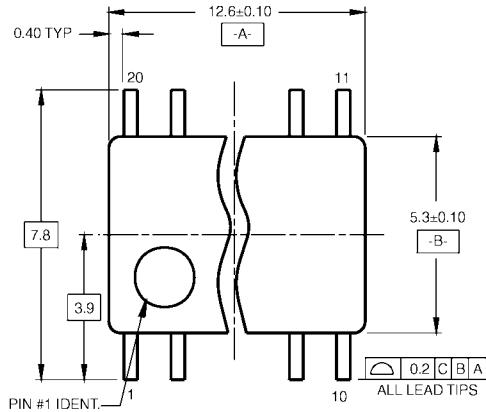
**Note 6:**  $C_{PD}$  determines the no load power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted

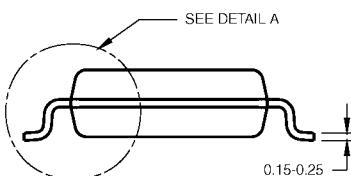
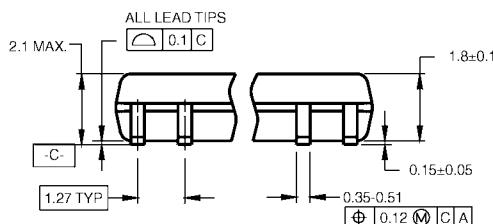


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B

## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION



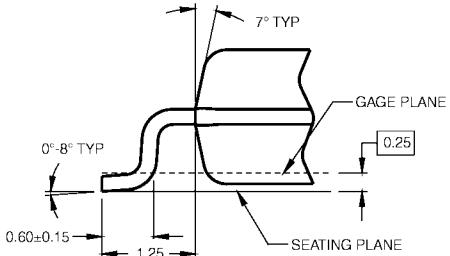
DIMENSIONS ARE IN MILLIMETERS

## NOTES:

NOTE:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

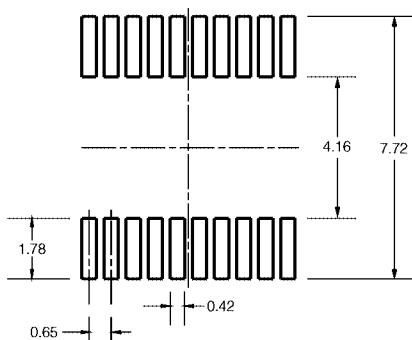
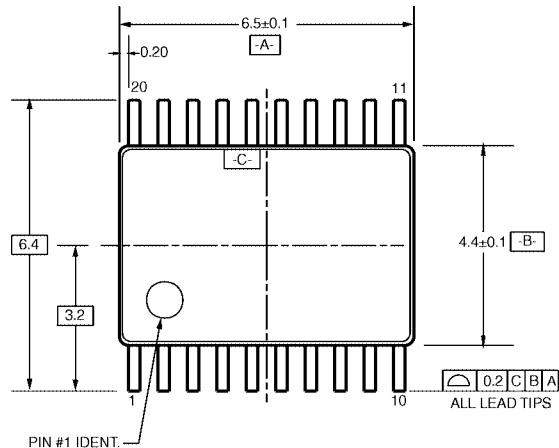
M20DRevB1



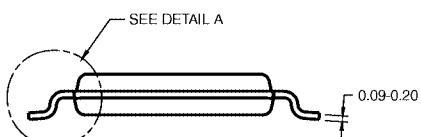
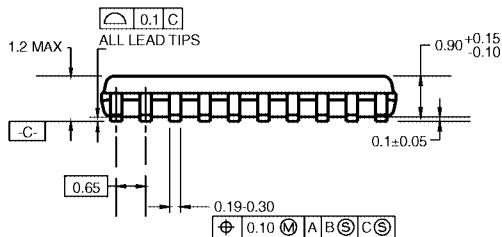
#### DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION

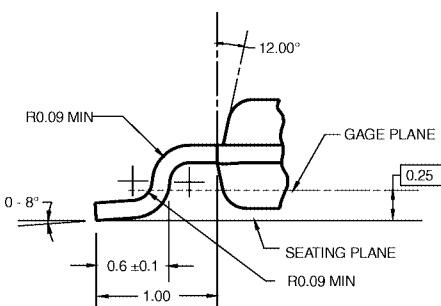


DIMENSIONS ARE IN MILLIMETERS

## NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

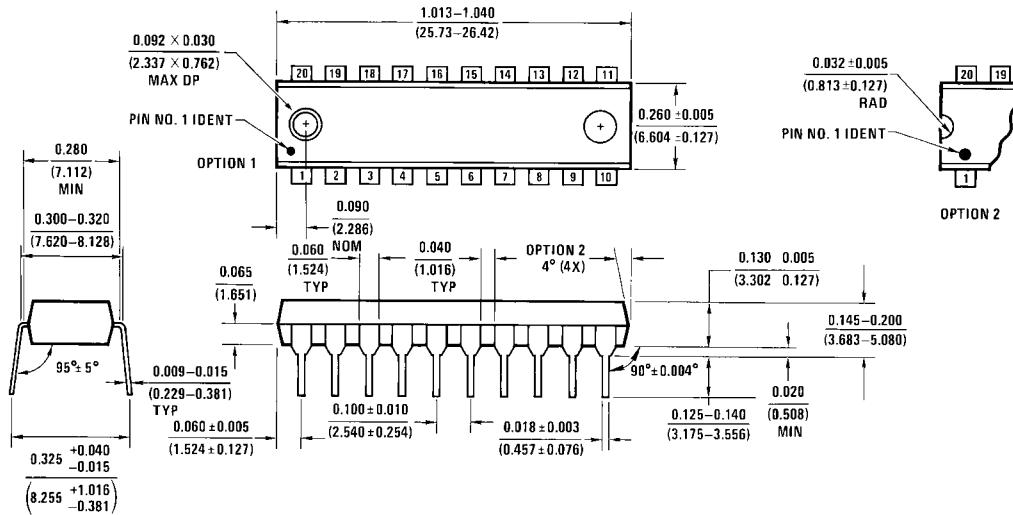
MTC20RevD1



## DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)