Jameco Part Number 42850

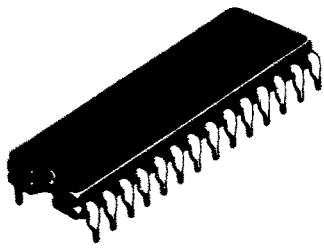
HM62256 Series

32768-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

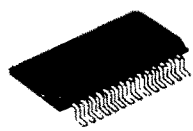
- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 200μW (typ)/10μW (typ) (L-version),
  Operation: 40mW (typ.) (f = 1MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/L-SL version)

HM62256P Series



(DP-28)

HM62256FP Series

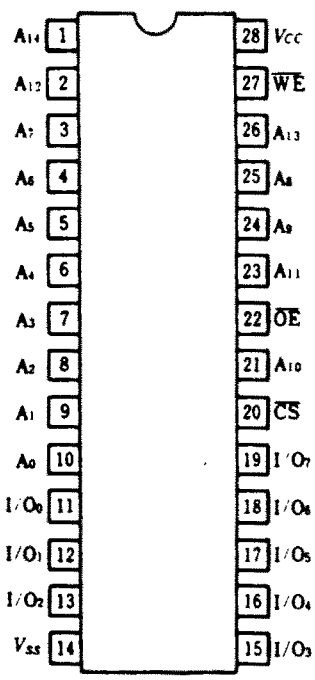


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62256P-8	85ns	600 mil 28 pin Plastic DIP
HM62256P-10	100ns	
HM62256P-12	120ns	
HM62256P-15	150ns	
HM62256LP-8	85ns	
HM62256LP-10	100ns	
HM62256LP-12	120ns	
HM62256LP-15	150ns	
HM62256LP-10SL	100ns	
HM62256LP-12SL	120ns	
HM62256LP-15SL	150ns	
HM62256FP-8T	85ns	28 pin Plastic SOP
HM62256FP-10T	100ns	
HM62256FP-12T	120ns	
HM62256FP-15T	150ns	
HM62256LFP-8T	85ns	
HM62256LFP-10T	100ns	
HM62256LFP-12T	120ns	
HM62256LFP-15T	150ns	
HM62256LFP-10SLT	100ns	
HM62256LFP-12SLT	120ns	
HM62256LFP-15SLT	150ns	

■ PIN ARRANGEMENT



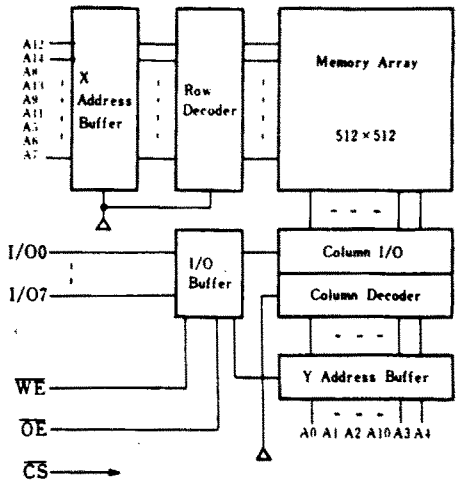
(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.0V for pulse width ≦ 50ns

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item		Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current		$\|I_{LI}\|$	$V_{IN} = V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current		$\|I_{LO}\|$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA	–	8	15	mA
Average Operating Power Supply Current	HM62256-8	I_{CC1}	Min. Cycle, duty = 100%, $\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA	–	50	70	mA
	HM62256-10			–	40	70	
	HM62256-12			–	35	70	
	HM62256-15			–	33	70	
		I_{CC2}	$\overline{CS} = V_{IL}$, $V_{IH} = V_{CC}$, V_{IL} = 0V, $I_{I/O}$ = 0mA, f = 1MHz	–	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS} = V_{IH}$	–	0.5	3	mA
		I_{SB1}	$\overline{CS} \geqq V_{CC}$ − 0.2V, 0V ≦ V_{IN}	–	0.04	2	mA
				–	2*2	100*2	μA
				–	2*3	50*3	
Output Voltage		V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
		V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V

Notes) *1. Typical values are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC}=5V± 10%, T_a=0 to +70°C unless otherwise noted)

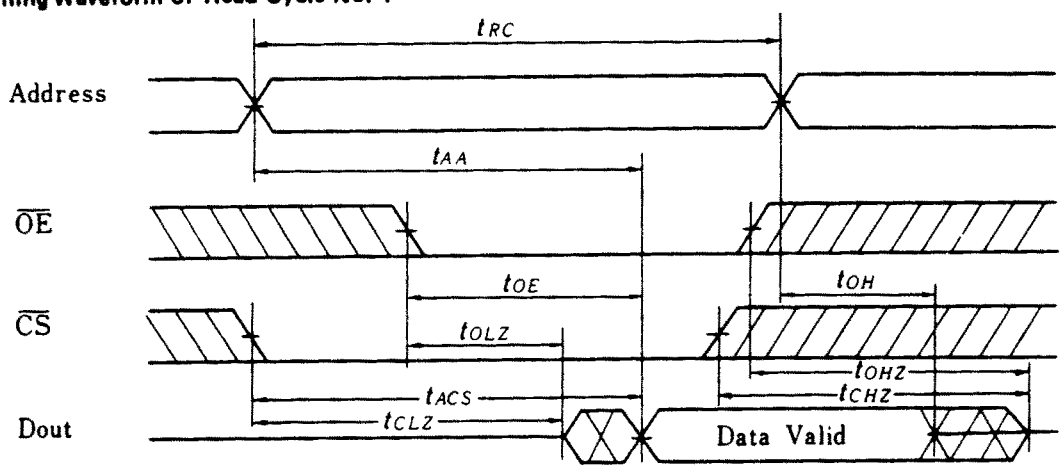
● AC Test Conditions

- ○ Input pulse levels: 0.8V to 2.4V
- ○ Input rise and fall times: 5ns
- ○ Input and Output timing reference levels: 1.5V
- ○ Output load: 1TTL Gate and C_L (100pF) (Including scope and jig)

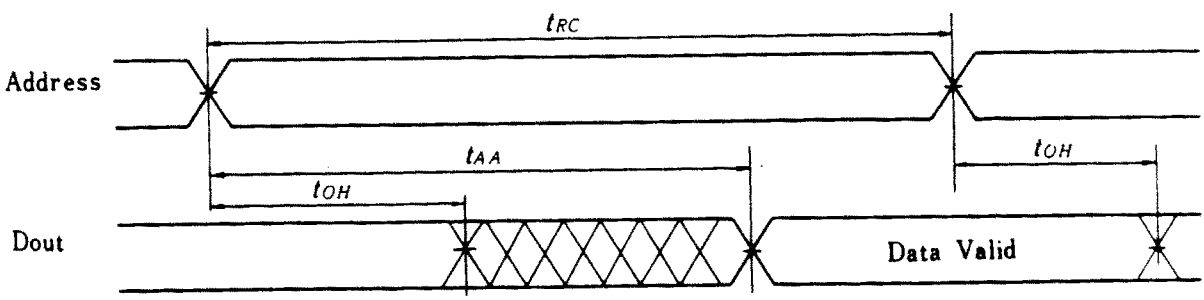
● Read Cycle

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	–	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	85	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	45	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

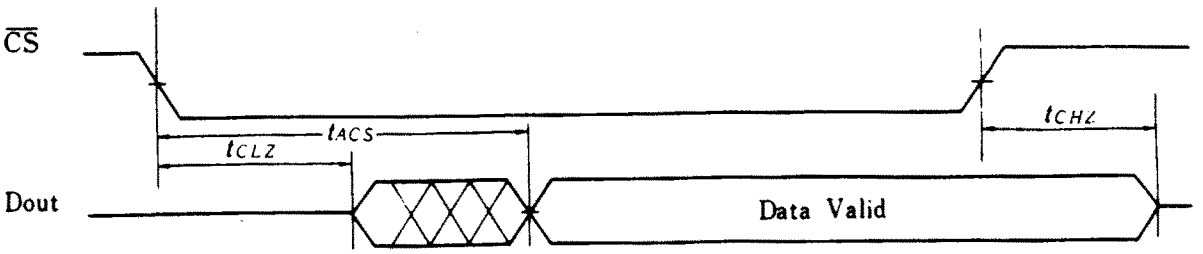
● Timing Waveform of Read Cycle No. 1[1]



● Timing Waveform of Read Cycle No. 2[1][2][4]



• Timing Waveform of Read Cycle No. 3[1][3][4]

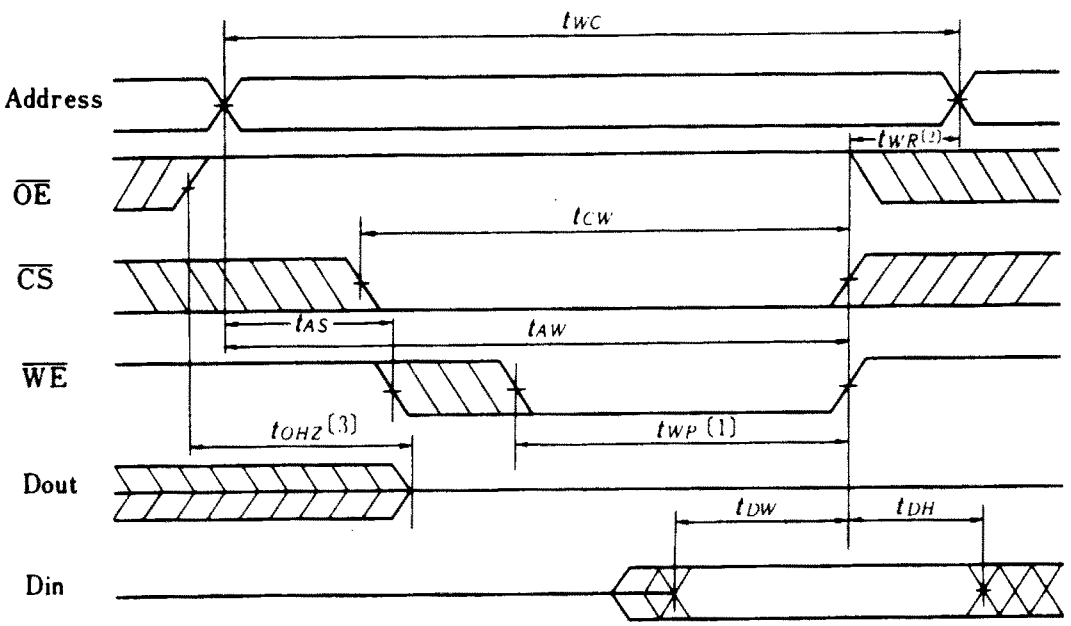


Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

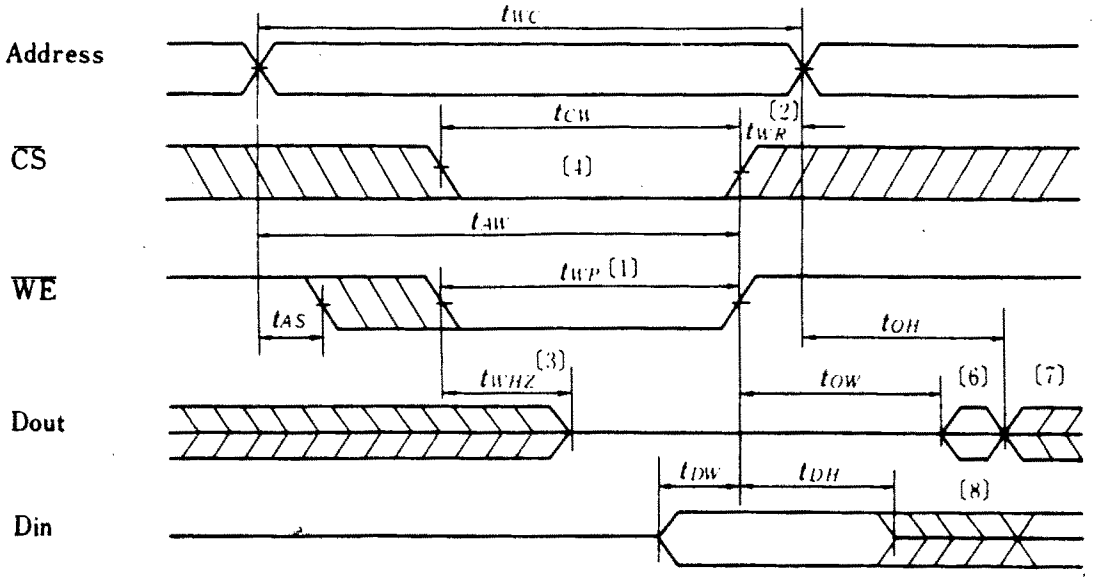
• Write Cycle

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	–	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	75	–	80	–	85	–	100	–	ns
Address Valid to End of Write	t_{AW}	75	–	80	–	85	–	100	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	60	–	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns

• Timing Waveform of Write Cycle No. 1 ($\overline{OE}$ Clock)



- **Timing Waveform of Write Cycle No. 2[5] ($\overline{OE}$ Low Fixed)**



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

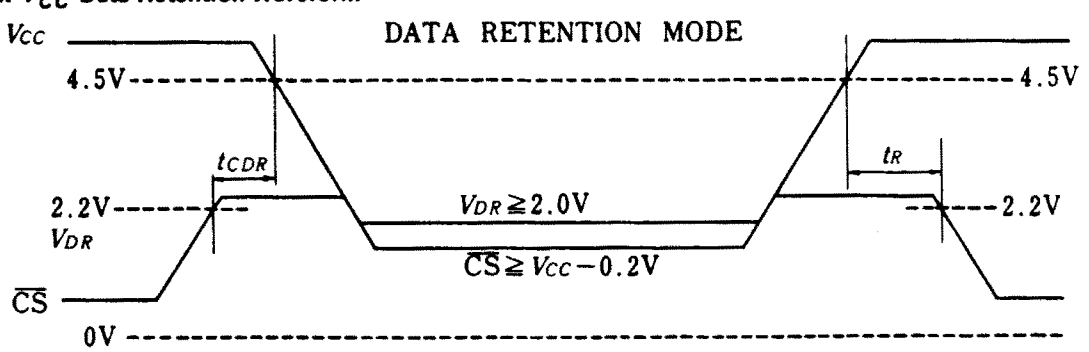
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

(This characteristics is guaranteed only for L-and L-SL version)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Date Retention	V_{DR}	$\overline{CS} \geqq V_{CC}$ −0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geqq$ 2.8V 0V ≦ V_{in}	–	–	50*2	μA
			–	–	10*3	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

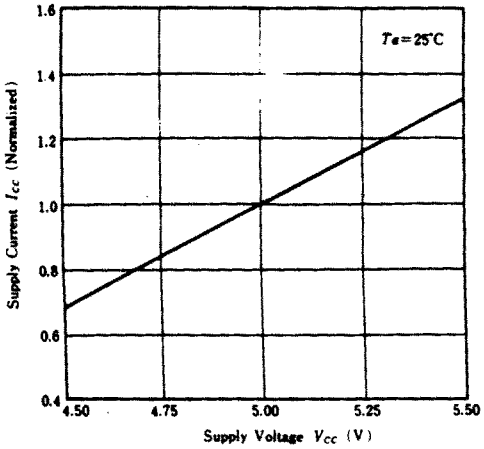
Note) *1. t_{RC} = Read Cycle Time
*2. This characteristic is guaranteed only for L-version, 20μA max. at T_a = 0 to 40°C.
*3. This characteristic is guaranteed only for L-SL version, 3μA max. at T_a = 0 to 40°C.

- **Low V_{CC} Data Retention Waveform**

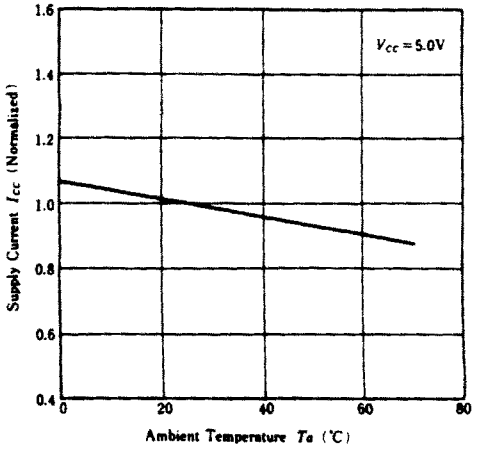


Note) In Data Retention Mode, $\overline{CS}$ controls the Address, $\overline{WE}$, $\overline{OE}$, and Din Buffers. *Vin* for these inputs can be in high impedance state in data retention mode.

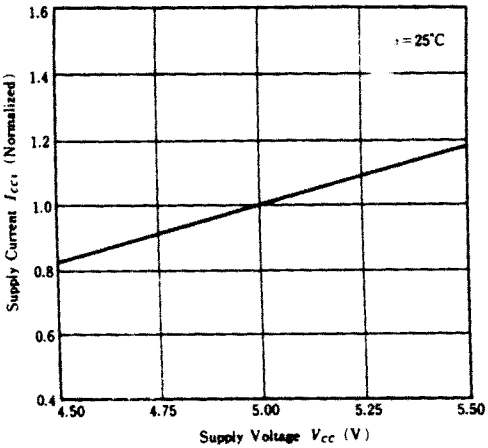
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1)



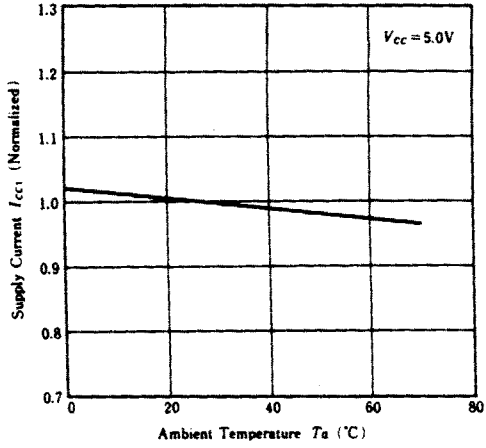
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (1)



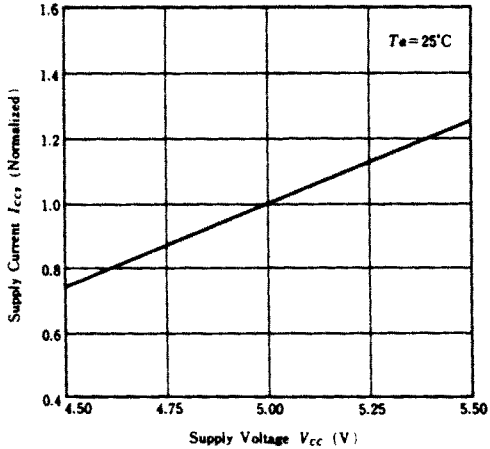
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2)



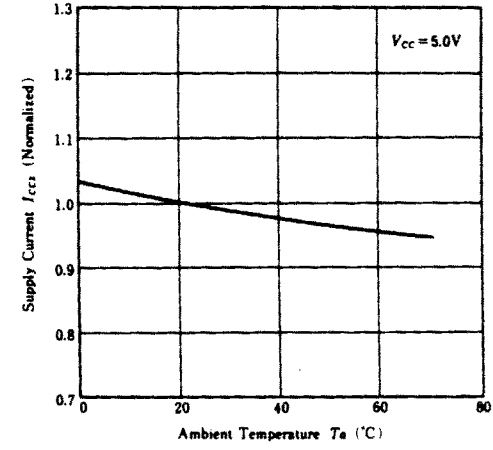
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (2)



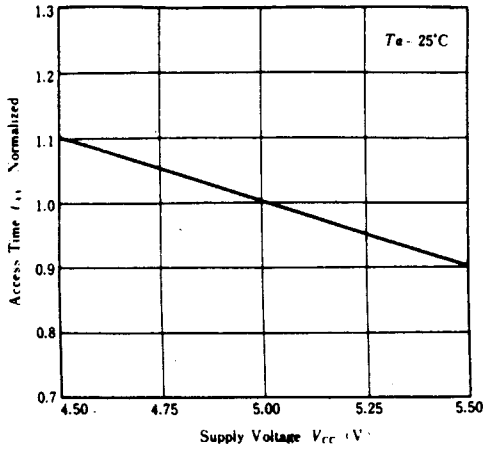
SUPPLY CURRENT vs. SUPPLY VOLTAGE (3)



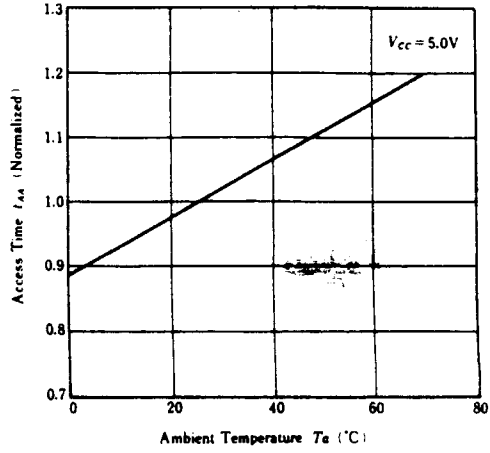
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (3)



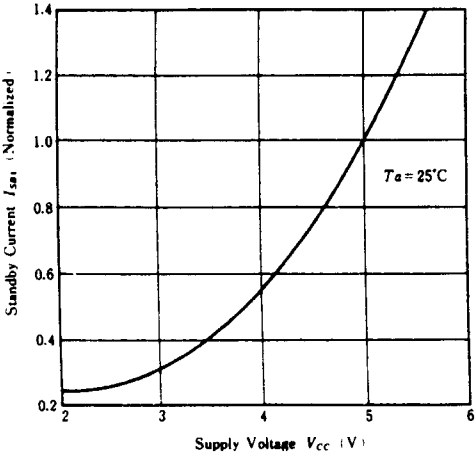
ACCESS TIME vs. SUPPLY VOLTAGE



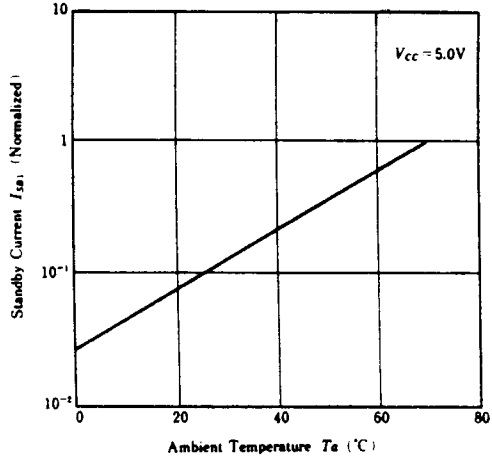
ACCESS TIME vs. AMBIENT TEMPERATURE



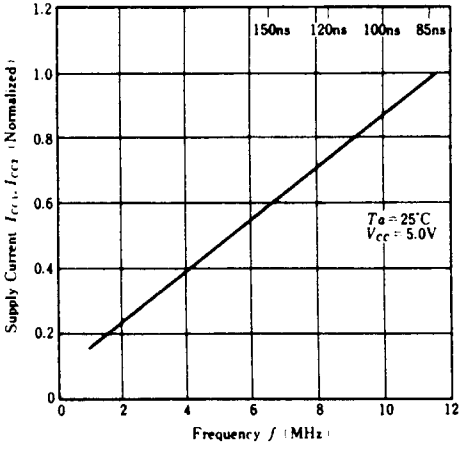
STANDBY CURRENT vs. SUPPLY VOLTAGE



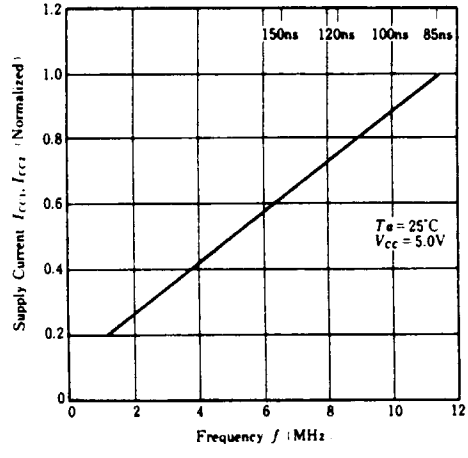
STANDBY CURRENT vs. AMBIENT TEMPERATURE



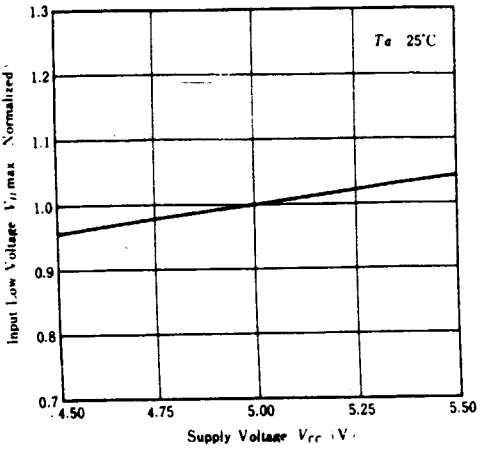
SUPPLY CURRENT vs. FREQUENCY (READ)



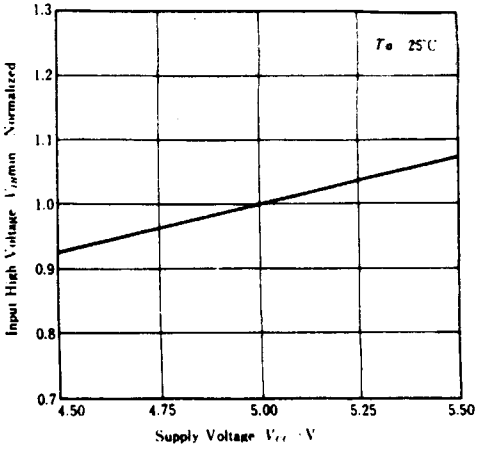
SUPPLY CURRENT vs. FREQUENCY (WRITE)



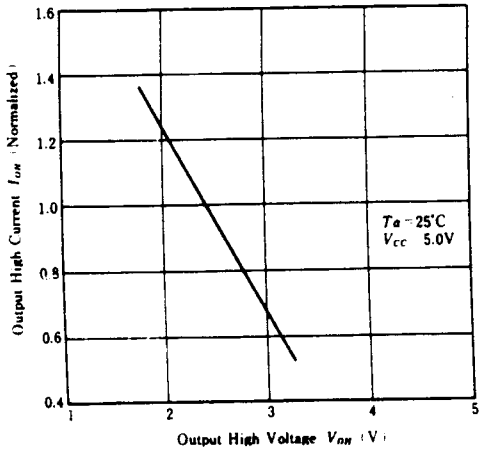
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



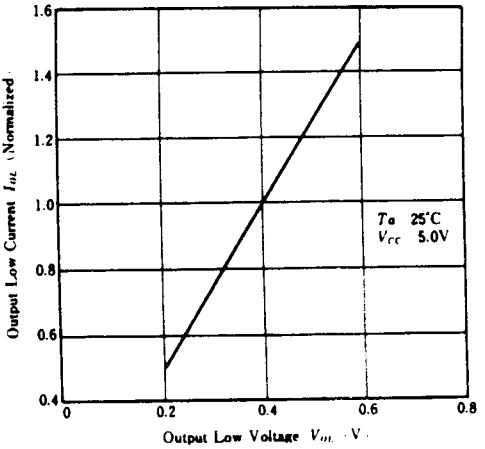
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME vs. LOAD CAPACITANCE