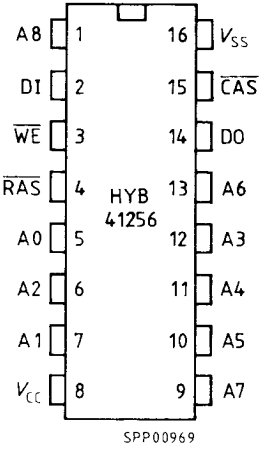
262,144-Bit Dynamic RAM

HYB 41256-10/-12/-15

- 262,144 × 1-bit organization
- Industry standard 16 pins
- Single + 5 V supply, ± 10 % tolerance
- Low power dissipation:
  – 358 mW active (max.)
  – 28 mW standby (max.)
- 100 ns access time
  200 ns cycle time (HYB 41256-10)
  120 ns access time
  220 ns cycle time (HYB 41256-12)
  150 ns access time
  260 ns cycle time (HYB 41256-15)
- All inputs and outputs TTL-compatible
- On-chip substrate bias generator
- Tristate data output
- Read, write, read-modify-write, $\overline{RAS}$-only refresh, hidden-refresh
- Common I/O capability using "early write" operation
- Page mode read and write, read-write
- 256 refresh cycles with 4 ms refresh period
- Redundancy incorporated for increasing yield – activation via laser links

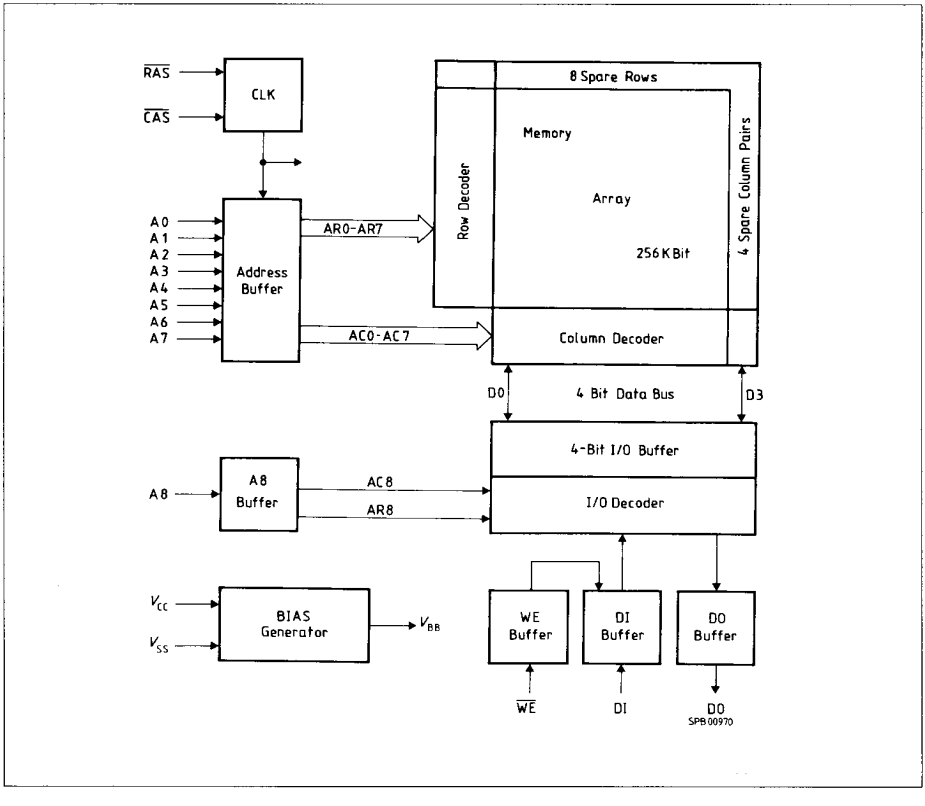
Pin Configuration



Pin Names

A0 – A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data Input
DO	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)

The HYB 41256 is a 262,144 word by 1-bit dynamic random access memory.
This 5 V-only component is fabricated with Siemens high-performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A low radiation molding compound protects the chip against soft errors.
Nine multiplexed address inputs permit the HYB 41256 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with ± 10 % tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL-compatible inputs and output, including clocks.
In addition to the usual read, write and read-modify-write cycles, the HYB 41256 is capable of early and late write cycles, $\overline{RAS}$-only refresh, and hidden refresh. Common I/O capability is given by using early write operation.
The HYB 41256 also features page mode which allows high-speed random access of bits in the same row.
The HYB 41256 has the capability of using laser links to perform redundancy.



Functional Description

Device Initialization

Since the HYB 41256 is a dynamic RAM with a single 5 V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the row address strobe ($\overline{RAS}$) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Addressing (A0 – A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits is required. First, 9 row address bits are set up on pins A0 through A8 and latched into the row address latches by the row address strobe ($\overline{RAS}$). Then, the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the column address strobe ($\overline{CAS}$). All input addresses must be stable on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. It should be noted that $\overline{RAS}$ is similar to a "chip enable" insofar as it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write Enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (V_{IH}) on $\overline{WE}$ dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data Output (DO)

The output is tristate TTL-compatible with a fan-out of two standard TTL loads. DO has the same polarity as DI. The output is in a high-impedance state until $\overline{CAS}$ is brought low. In a read cycle or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (min.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. With $\overline{CAS}$ going high the output returns to the high-impedance state within t_{OFF}.

Hidden refresh

$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as hidden refresh. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$, causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Page mode

Page-mode operation allows effectively faster memory access by maintaining the row address and strobing random column addresses on the chip. Thus, the time necessary to setup and strobe sequential row addresses for the same page is no longer required. The maximum number of columns that can be addressed in sequence is determined by t_{RAS}, the maximum $\overline{RAS}$ low pulse width.

Absolute Maximum Ratings

Operating temperature range	0 to + 70 °C
Storage temperature range	– 65 to + 150 °C
Voltage on any pin relative to V_{SS}	– 1 to 7 V
Power dissipation	1 W
Data output current (short circuit)	50 mA

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{CC} = + 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage (all inputs)	2.4	V_{CC} + 1	V	2) 3)
V_{IL}	Input low voltage (all inputs)	– 1.0	0.8	V	2) 3)
V_{OH}	Output high voltage	2.4	–	V	7)
V_{OL}	Output low voltage	–	0.4	V	8)
I_{CC1}	Average V_{CC} supply current – 10 t_{RC} = 200 ns – 12 t_{RC} = 220 ns – 15 t_{RC} = 260 ns	–	 85 75 65	mA	4)
I_{CC2}	Standby V_{CC} supply current	–	5	mA	5)
I_{CC3}	Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles – 10 t_{RC} = 200 ns – 12 t_{RC} = 220 ns – 15 t_{RC} = 260 ns	–	 70 60 50	mA	4)
I_{CC4}	Average V_{CC} supply current during page mode – 10 t_{PC} = 100 ns – 12 t_{PC} = 120 ns – 15 t_{PC} = 150 ns	–	 70 60 50	mA	4)
$I_{I(L)}$	Input leakage current (any input)	– 10	10	µA	–
$I_{O(L)}$	Output leakage current ($\overline{CAS}$ at logic 1, 0 ≤ Vout ≤ 5.5)	– 10	10	µA	–
V_{CC}	V_{CC} supply voltage	4.5	5.5	V	2)
V_{SS}	V_{SS} supply voltage	0	0	V	2)

Notes see page 40.

Capacitance

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{I1}	Input capacitance (A0 – A8, DI)	–	7	pF	6)
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	–	7	pF	6)
C_O	Output capacitance (DO, $\overline{CAS}$ = V_{IH} to disable output)	–	7	pF	6)

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) All voltages refered to V_{SS}.

3) Overshooting and undershooting on input levels of 6.5 V or – 2 V for a period of 30 ns max. will not influence function and reliability of the device.

4) I_{CC} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

5) $\overline{RAS}$ and $\overline{CAS}$ are both V_{IH}.

6) Effective capacitance calculated from the equation. $C = \frac{I \cdot \Delta t}{\Delta V}$ with ΔV = 3 V or measured with Boonton meter.

7) I_{OH} = – 5.0 mA

8) I_{OL} = + 4.2 mA

AC Test Conditions

Input pulse levels		0 to 3.0 V
Input rise and fall times	5 ns between	0.8 and 2.4 V
Input timing reference levels		0.8 to 2.4 V
Output timing reference levels		0.4 to 2.4 V
Output load		equivalent to 2 standard TTL loads and 100 pF

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = + 5 V ± 10 % (unless otherwise specified; see notes 9, 10, 11)

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		– 10		– 12		– 15		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time [12]	200	–	220	–	260	–	ns
t_{RWC}	Read-modify-write cycle time [12]	235	–	265	–	310	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [13] [14]	–	100	–	120	–	150	ns
t_{CAC}	Access time from $\overline{CAS}$ [13] [15]	–	50	–	60	–	75	ns
t_{RAS}	$\overline{RAS}$ pulse width	100	10^4	120	10^4	150	10^4	ns
t_{CAS}	$\overline{CAS}$ pulse width	50	–	60	–	75	–	ns
t_{REF}	Refresh period	–	4	–	4	–	4	ms
t_{RP}	$\overline{RAS}$ precharge time	90	–	90	–	100	–	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0	–	0	–	0	–	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [16]	25	50	30	60	30	75	ns
t_{RSH}	$\overline{RAS}$ hold time	50	–	60	–	75	–	ns
t_{CSH}	$\overline{CAS}$ hold time	100	–	120	–	150	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	15	–	20	–	20	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	20	–	30	–	30	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$ [17]	70	–	90	–	105	–	ns
t_T	Transition time (rise and fall) [9]	3	50	3	50	3	50	ns
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time referenced to $\overline{CAS}$ [18]	0	–	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [18]	10	–	10	–	10	–	ns
t_{OFF}	Output buffer turn-off delay [19]	0	30	0	30	0	40	ns
t_{WCS}	Write command setup time [20]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	35	–	40	–	45	–	ns

Notes see page 42.

AC Characteristics (cont'd)

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		– 10		– 12		– 15		
		min.	max.	min.	max.	min.	max.	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$ [17]	100	–	100	–	120	–	ns
t_{WP}	Write command pulse width	30	–	40	–	45	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	30	–	40	–	45	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	30	–	40	–	45	–	ns
t_{DS}	Data in setup time [21]	0	–	0	–	0	–	ns
t_{DH}	Data in hold time [21]	30	–	40	–	45	–	ns
t_{DHR}	Data in hold time referenced to $\overline{RAS}$ [17]	90	–	100	–	120	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay [20]	50	–	60	–	75	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay [20]	100	–	120	–	150	–	ns
t_{RRW}	RMW cycle $\overline{RAS}$ pulse width	140	–	165	–	200	–	ns
t_{CRW}	RMW cycle $\overline{CAS}$ pulse width	85	–	105	–	125	–	ns
t_{PC}	Page mode cycle time [12]	100	–	120	–	145	–	ns
t_{PRWC}	Page mode read-write cycle time	130	–	160	–	190	–	ns
t_{CP}	Page mode $\overline{CAS}$ precharge time	40	–	50	–	60	–	ns

9) V_{IH} and V_{IL} are reference levels to measure timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10) An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.

11) The time parameters specified here are valid for a transition time of t_T = 5 ns for the input signals.

12) The specification for t_{RC} (min.), t_{RWC} (min.), and page-mode cycle time (t_{PC}) are only used to indicate cycle time at which proper operation over full temperature range (0 °C ≤ T_A ≤ 70 °C) is assured.

13) Measured with a load equivalent to two TTL loads and 100 pF.

14) Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

15) Assumes that $t_{RCD} \geq t_{RCD}$ (max.).

16) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

17) $t_{RCD} + t_{CAH} \geq t_{AR}$ min., $t_{RCD} + t_{DH} \geq t_{DHR}$ min., $t_{RCD} + t_{WCH} \geq t_{WCR}$ min.

18) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

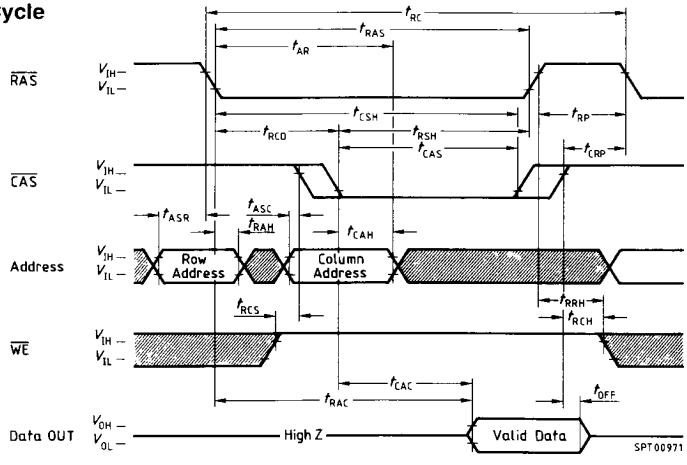
19) t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

20) t_{WCS}, t_{CWD} and t_{RWC} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open-circuit (high-impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.

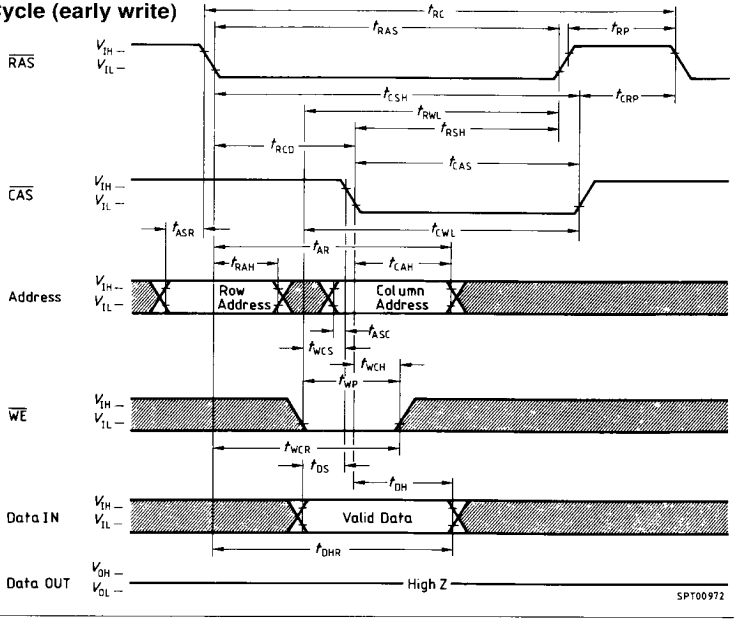
21) t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write of read-modify-write cycles.

Waveforms

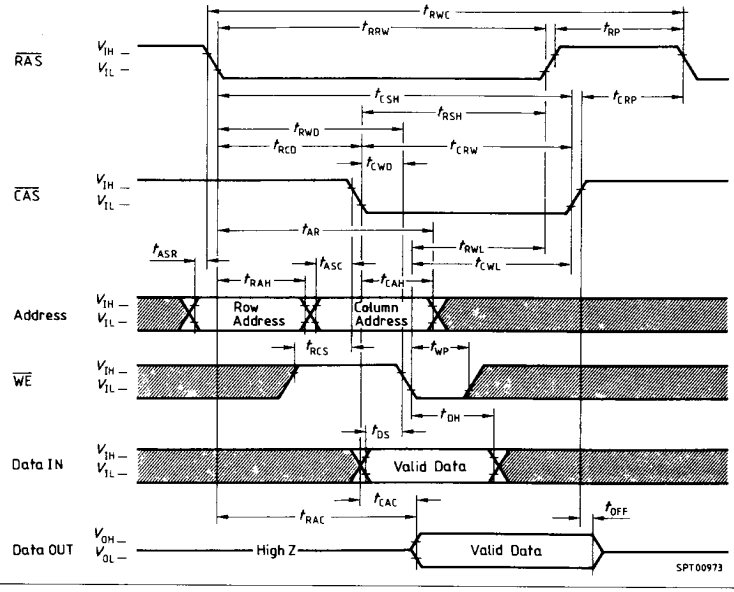
Read Cycle



Write Cycle (early write)

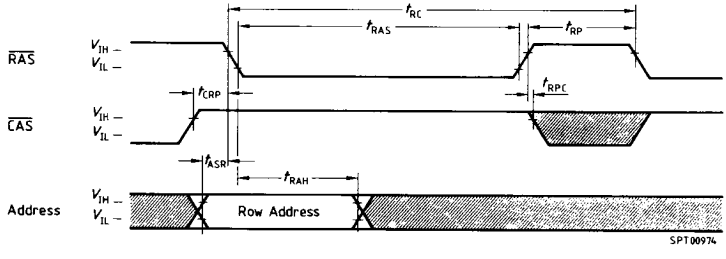


Read-Modify-Write or Late Write Cycle

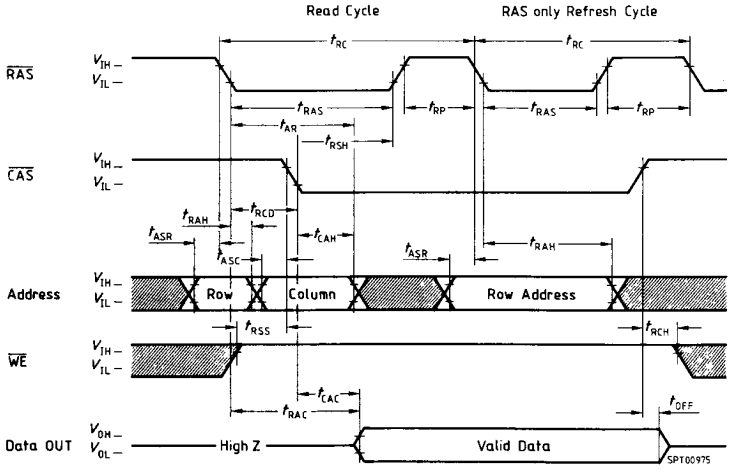


$\overline{RAS}$-Only Refresh Cycle

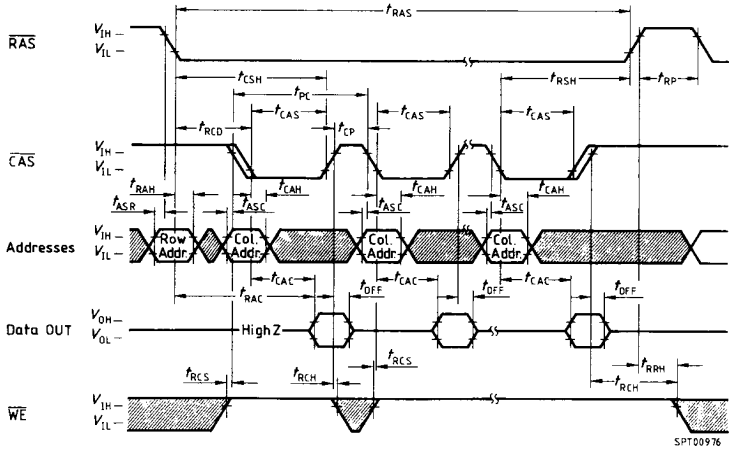
(DI and $\overline{WE}$ = don't care)



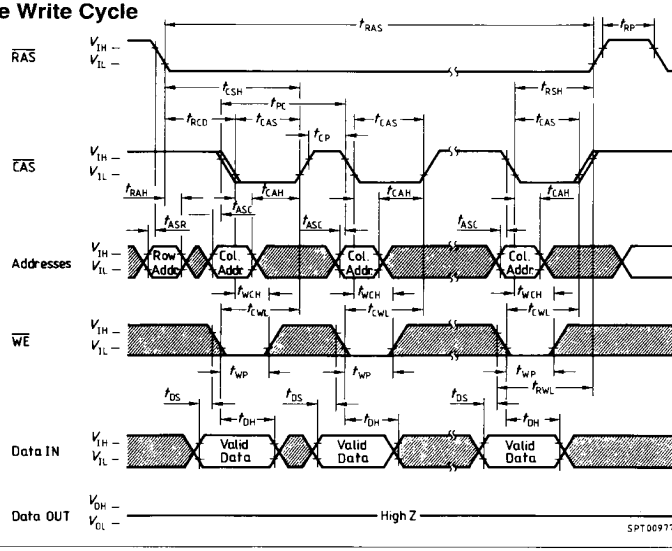
Hidden Refresh Cycle



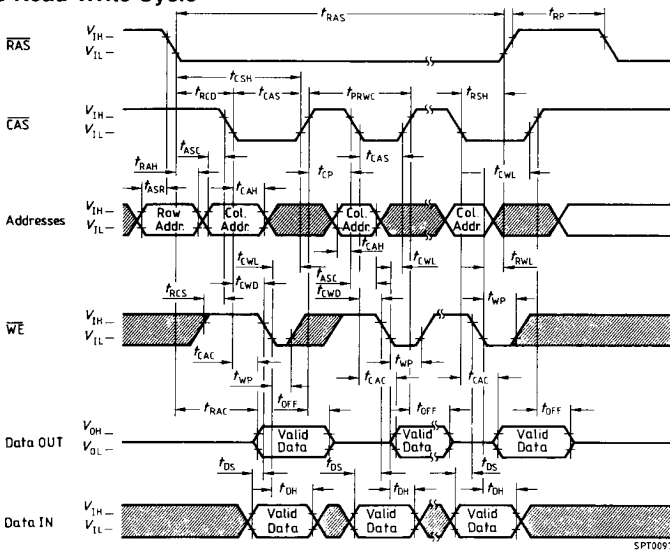
Page-Mode Read Cycle



Page-Mode Write Cycle



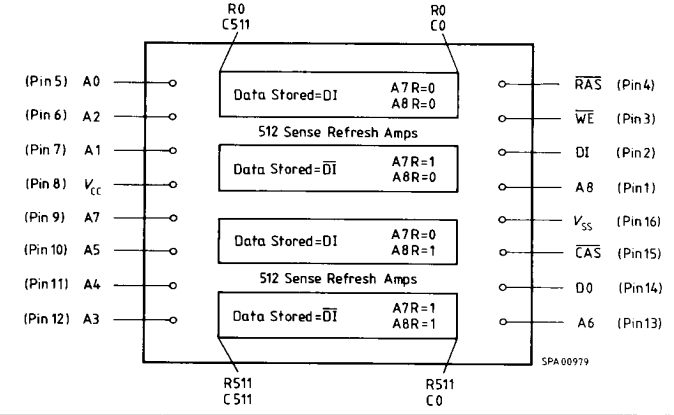
Page-Mode Read-Write Cycle



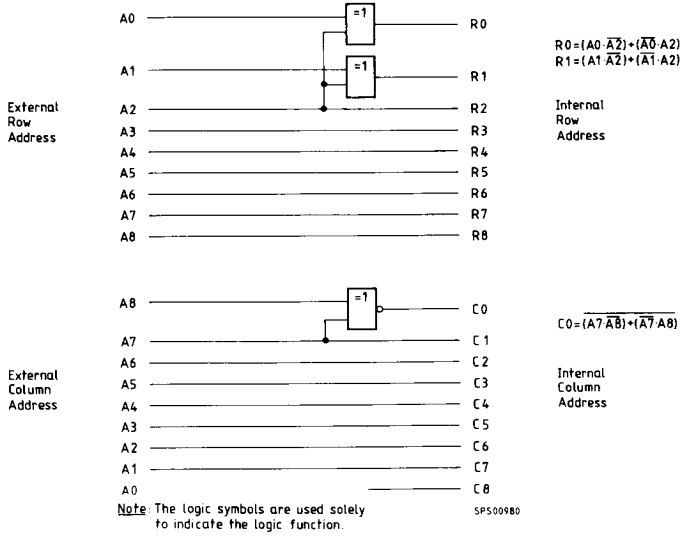
Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal address scrambling of the device in order to check for 'worst case' pattern.

Internal Address Scrambling



Address Decoder Scrambling



Redundancy

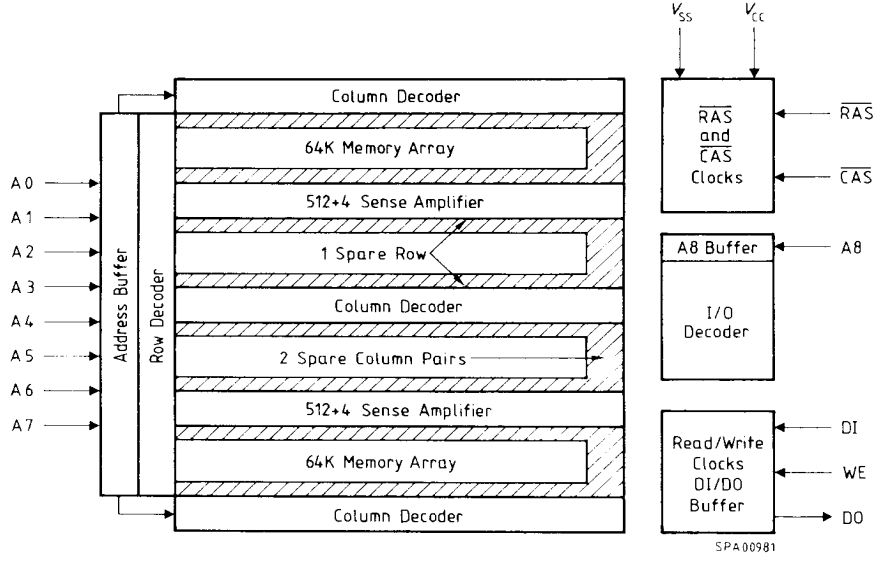
Redundancy Concept

The HYB 41256 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser Technology

For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blowup of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip area.

Siemens 256K DRAM Chip Topology



Ordering Information

Type	Ordering code	Description
HYB 41256-10	Q67100-Q380	DRAM (access time 100 ns)
HYB 41256-12	Q67100-Q346	DRAM (access time 120 ns)
HYB 41256-15	Q67100-Q347	DRAM (access time 150 ns)