

# SN54283, SN54LS283, SN54S283, SN74283, SN74LS283, SN74S283 4-BIT BINARY FULL ADDERS WITH FAST CARRY

SDLS095A - OCTOBER 1976 - REVISED MARCH 1988

- Full-Carry Look-Ahead Across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

## TYPICAL ADD TIMES

TYPE	TWO 8-BIT WORDS	TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER ADDER
'283	23ns	43ns	310 mW
'LS283	25ns	45ns	95 mW
'S283	15ns	30ns	510 mW

## description

The '283 and 'LS283 adders are electrically and functionally identical to the '83A and 'LS83A, respectively; only the arrangement of the terminals has been changed. The 'S283 high performance versions are also functionally identical.

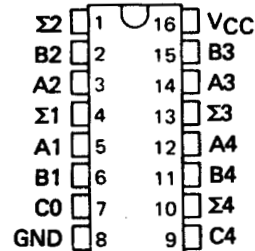
These improved full adders perform the addition of two 4-bit binary words. The sum ( $\Sigma$ ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look-ahead across all four bits generating the carry term in ten nanoseconds, typically, for the '283 and 'LS283, and 7.5 nanoseconds for the 'S283. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Series 74, Series 74LS, and Series 74S circuits are characterized for  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  operation.

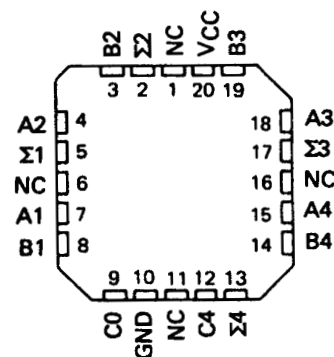
SN54283, SN54LS283 . . . J OR W PACKAGE  
SN54S283 . . . J PACKAGE  
SN74283 . . . N PACKAGE  
SN74LS283, SN74S283 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS283, SN54S283 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

## FUNCTION TABLE

INPUT				OUTPUT							
				WHEN C0 = L				WHEN C0 = H			
				WHEN C2 = L				WHEN C2 = H			
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2	Σ3	C4
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4	Σ4	C4
L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	L
L	H	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	L
L	H	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L
H	L	L	H	L	L	L	L	L	L	L	L
H	L	H	L	L	L	L	L	L	L	L	L
H	L	H	H	L	L	L	L	L	L	L	L
H	H	L	L	L	L	L	L	L	L	L	L
H	H	L	H	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	L	L	L	L	L
H	H	H	H	L	L	L	L	L	L	L	L

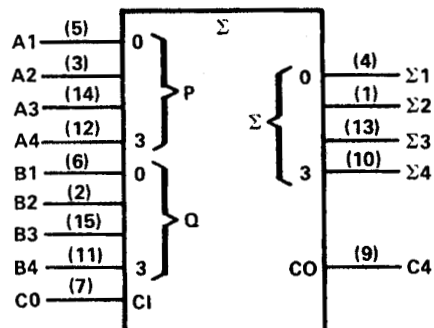
H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

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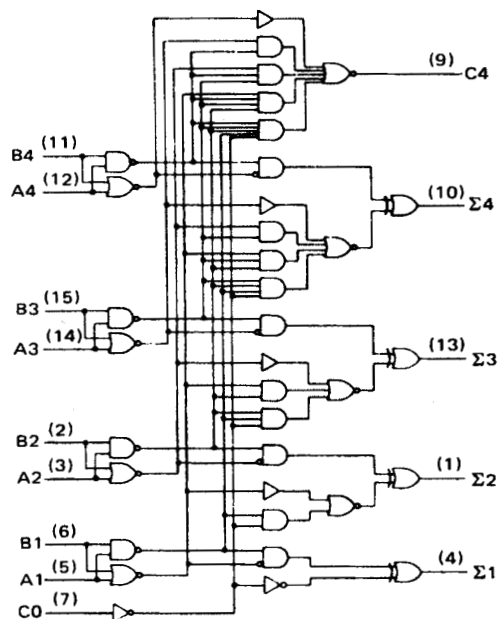
## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

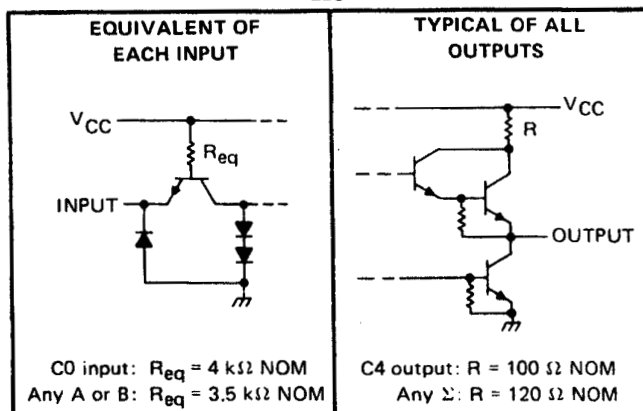
Pin numbers shown are for D, J, N, and W packages.

## logic diagram (positive logic)

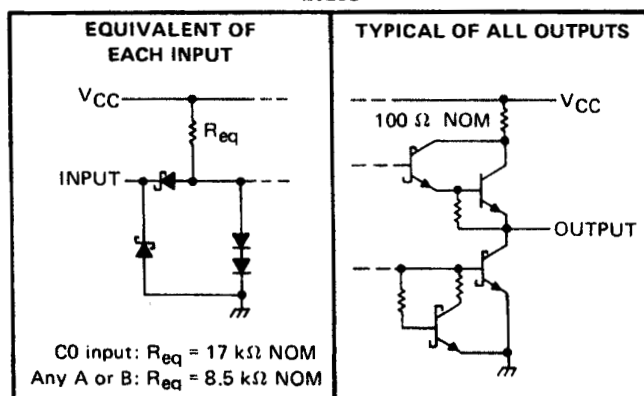


Pin numbers shown are for D, J, N, and W packages.

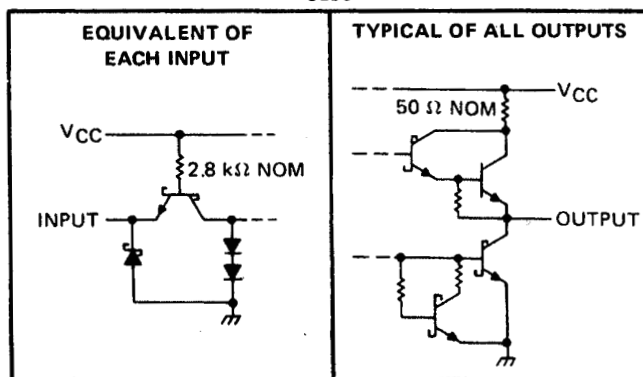
## schematics of inputs and outputs '283



## 'LS283



## 'S283



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7V
Input voltage: '283, 'S283	5.5V
'LS283	7V
Interemitter voltage (see Note 2)	5.5V
Operating free-air temperature range: SN54283, SN54LS283, SN54S283	-55°C to 125°C
SN74283, SN74LS283, SN74S283	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '283 and 'S283 only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

# SN54283, SN74283

## 4-BIT BINARY FULL ADDERS WITH FAST CARRY

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### recommended operating conditions

			SN54283			SN74283			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V <sub>CC</sub>			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I <sub>OH</sub>	Any output except C4		-800			-800			μA
	Output C4		-400			-400			
Low-level output current, I <sub>OL</sub>	Any output except C4		16			16			mA
	Output C4		8			8			
Operating free-air temperature, T <sub>A</sub>			-55			0			70 °C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54283			SN74283			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage				2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			0.8			V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA		-1.5			-1.5			V
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX		2.4	3.6		2.4	3.6		V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = MAX			0.2	0.4		0.2	0.4	V
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1			1			mA
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		40			40			μA
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-1.6			-1.6			mA
I <sub>OS</sub>	Short-circuit output current §	Any output except C4	V <sub>CC</sub> = MAX		-20		-55	-18		-55	mA
		Output C4			-20		-70	-18		-70	
I <sub>CC</sub>	Supply current		V <sub>CC</sub> = MAX, Outputs open	All B low, other inputs at 4.5 V	56		56		mA		
				All inputs at 4.5 V	66 99		66 110				

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Only one output should be shorted at a time.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER <sup>¶</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	C0	Any Σ	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Note 3	14	21	ns	
t <sub>PHL</sub>				12	21		
t <sub>PLH</sub>	A <sub>i</sub> or B <sub>i</sub>	Σ <sub>i</sub>		16	24	ns	
t <sub>PHL</sub>				16	24		
t <sub>PLH</sub>	C0	C4	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 780 Ω, See Note 3	9	14	ns	
t <sub>PHL</sub>				11	16		
t <sub>PLH</sub>	A <sub>i</sub> or B <sub>i</sub>	C4		9	14	ns	
t <sub>PHL</sub>				11	16		

<sup>¶</sup>  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN54LS283, SN74LS283

## 4-BIT BINARY FULL ADDERS WITH FAST CARRY

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### recommended operating conditions

	SN54LS283			SN74LS283			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS283			SN74LS283			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$	High-level input voltage		2			2			V
$V_{IL}$	Low-level input voltage				0.7			0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
$I_I$	Input current at maximum input voltage	Any A or B		0.2			0.2		mA
		C0		0.1			0.1		
$I_{IH}$	High-level input current	Any A or B		40			40		$\mu$ A
		C0		20			20		
$I_{IL}$	Low-level input current	Any A or B		-0.8			-0.8		mA
		C0		-0.4			-0.4		
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
$I_{CC}$	Supply current	All inputs grounded	22	39		22	39		mA
		All B low, other inputs at 4.5 V	19	34		19	34		
		All inputs at 4.5 V	19	34		19	34		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Only one output should be shorted at a time and duration of the short-circuit should not exceed one second.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	C0	Any Σ	CL = 15 pF, See Note 3RL = 2 kΩ,		16	24	ns	
tPHL					15	24		
tPLH	Ai or Bi	Σi			15	24	ns	
tPHL					15	24		
tPLH	C0	C4			11	17	ns	
tPHL					11	22		
tPLH	Ai or Bi	C4			11	17	ns	
tPHL					12	17		

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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# SN54S283, SN74S283

## 4-BIT BINARY FULL ADDERS WITH FAST CARRY

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### recommended operating conditions

		SN54S283			SN74S283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	Any output except C4	-1			-1			mA
	Output C4	-500			-500			$\mu$ A
Low-level output current, $I_{OL}$	Any output except C4	20			20			mA
	Output C4	10			10			
Operating free-air temperature, $T_A$		-55			0			$^{\circ}$ C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{IH}$	High-level input voltage			2			V
$V_{IL}$	Low-level input voltage					0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$				-1.2	V
$V_{OH}$	High-level output voltage	SN54S283	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,	2.5	3.4		V
		SN74S283	$V_{IL} = 0.8 \text{ V}$ , $I_{OH} = \text{MAX}$	2.7	3.4		
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = \text{MAX}$				0.5	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$				1	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$				50	$\mu$ A
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.5 \text{ V}$				-2	mA
$I_{OS}$	Short-circuit output current§	Any output except C4	$V_{CC} = \text{MAX}$	-40		-100	mA
		Output C4		-20		-100	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , Outputs open	All B low, other inputs at 4.5 V		80		mA
			All inputs at 4.5 V		95	160	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	C0	Any Σ	CL = 15 pF, RL = 280 Ω, See Note 3		11	18	ns
tPHL					12	18	
tPLH	Ai or Bi	Σi			12	18	ns
tPHL					11.5	18	
tPLH	C0	C4	CL = 15 pF, RL = 560 Ω, See Note 3		6	11	ns
tPHL					7.5	11	
tPLH	Ai or Bi	C4			7.5	12	ns
tPHL					8.5	12	

†  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7604301VEA	ACTIVE	CDIP	J	16	25	TBD	A42	N / A for Pkg Type		5962-7604301VE A SNV54LS283J	<a href="#">Samples</a>
76043012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76043012A SNJ54LS 283FK	<a href="#">Samples</a>
7604301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604301EA SNJ54LS283J	<a href="#">Samples</a>
7604301FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604301FA SNJ54LS283W	<a href="#">Samples</a>
JM38510/31202B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 31202B2A	<a href="#">Samples</a>
JM38510/31202BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31202BEA	<a href="#">Samples</a>
JM38510/31202BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31202BFA	<a href="#">Samples</a>
M38510/31202B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 31202B2A	<a href="#">Samples</a>
M38510/31202BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31202BEA	<a href="#">Samples</a>
M38510/31202BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 31202BFA	<a href="#">Samples</a>
SN54LS283J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS283J	<a href="#">Samples</a>
SN54S283J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S283J	<a href="#">Samples</a>
SN74283N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS283D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS283	<a href="#">Samples</a>
SN74LS283DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS283	<a href="#">Samples</a>
SN74LS283DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS283	<a href="#">Samples</a>
SN74LS283N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS283N	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS283N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS283NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS283N	<a href="#">Samples</a>
SN74LS283NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS283	<a href="#">Samples</a>
SN74LS283NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS283	<a href="#">Samples</a>
SN74LS283NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS283	<a href="#">Samples</a>
SN74S283D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74S283N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S283N	<a href="#">Samples</a>
SN74S283N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S283NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S283N	<a href="#">Samples</a>
SNJ54LS283FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76043012A SNJ54LS 283FK	<a href="#">Samples</a>
SNJ54LS283J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604301EA SNJ54LS283J	<a href="#">Samples</a>
SNJ54LS283W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7604301FA SNJ54LS283W	<a href="#">Samples</a>
SNJ54S283FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 283FK	<a href="#">Samples</a>
SNJ54S283J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S283J	<a href="#">Samples</a>
SNJ54S283W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S283W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54283, SN54LS283, SN54LS283-SP, SN54S283, SN74283, SN74LS283, SN74S283 :**

● Catalog: [SN74283](#), [SN74LS283](#), [SN54LS283](#), [SN74S283](#)

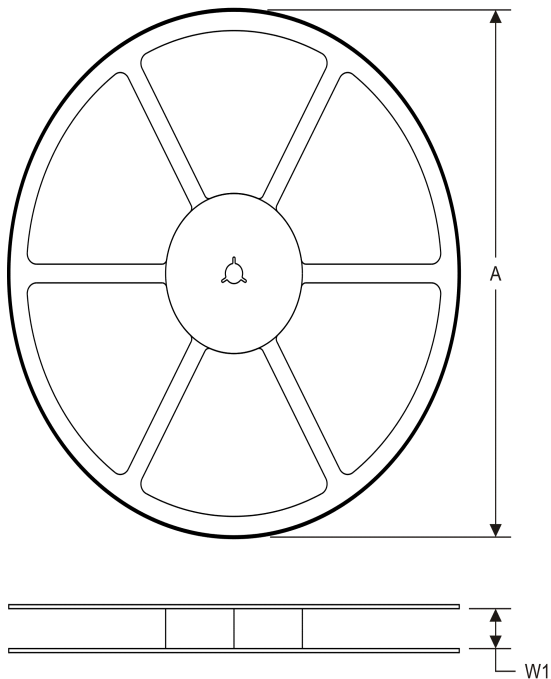
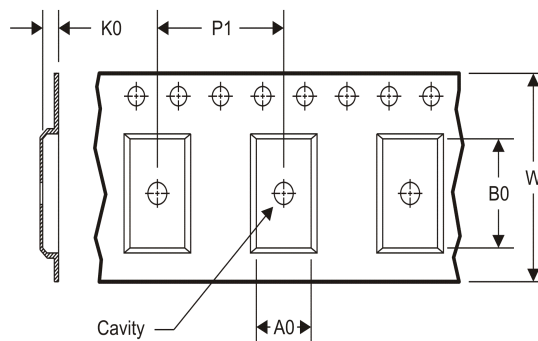
● Military: [SN54283](#), [SN54LS283](#), [SN54S283](#)

● Space: [SN54LS283-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS283NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS283NSR	SO	NS	16	2000	367.0	367.0	38.0

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