Jameco Part Number 13186TI

TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS051A – Revised March 2002

# CD4066B Types

## CMOS Quad Bilateral Switch

### For Transmission or Multiplexing of Analog or Digital Signals

### High-Voltage Types (20-Volt Rating)

■ CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

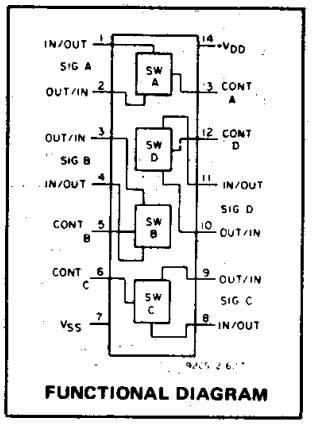
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig.1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to $V_{SS}$ when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

*Features:*

- 15-V digital or ±7.5-V peak-to-peak switching
- 125Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 5 Ω over 15-V signal-input range
- On-state resistance flat over full peak-to-peak signal range
- High on/off output-voltage ratio: 80 dB typ. @ $f_{is}$ = 1 kHz, $R_L$ = 1 kΩ
- High degree of linearity: <0.5% distortion typ. @ $f_{is}$ = 1 kHz, $V_{is}$ = 5 Vp-p, $V_{DD} - V_{SS} \geq 10$ V, $R_L$ = 10 kΩ
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, $T_A$ = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): $10^{12}$ Ω typ.
- Low crosstalk between switches: –50 dB typ. @ $f_{is}$ = 8 MHz, $R_L$ = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"



FUNCTIONAL DIAGRAM

*Applications:*

- Analog signal switching/multiplexing
  Signal gating — Modulator
  Squelch control — Demodulator
  Chopper — Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

**MAXIMUM RATINGS, *Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

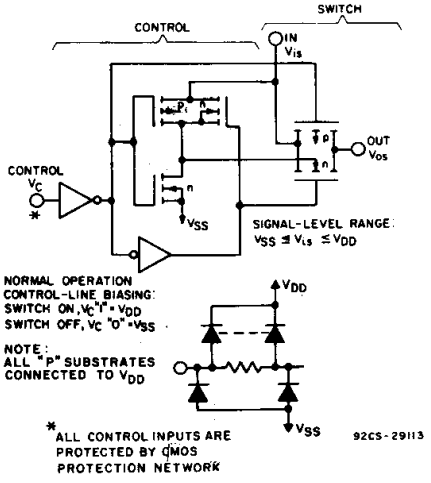



*Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.*

**RECOMMENDED OPERATING CONDITIONS**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | 3 | 18 | V |

## ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | TEST CONDITIONS | $V_{IN}$ (V) | $V_{DD}$ (V) | LIMITS AT INDICATED TEMPERATURES (°C) −55 | −40 | +85 | +125 | +25 Typ. | +25 Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| Quiescent Device Current, $I_{DD}$ | | 0,5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | 0.01 | 0.25 | μA |
| | | 0,10 | 10 | 0.5 | 0.5 | 15 | 15 | 0.01 | 0.5 | |
| | | 0,15 | 15 | 1 | 1 | 30 | 30 | 0.01 | 1 | |
| | | 0,20 | 20 | 5 | 5 | 150 | 150 | 0.02 | 5 | |
| **Signal Inputs ($V_{is}$) and Output ($V_{os}$)** | | | | | | | | | | |
| On-State Resistance, $r_{on}$ Max. | $V_C = V_{DD}$, $R_L$ = 10 kΩ returned to $\frac{V_{DD}-V_{SS}}{2}$, $V_{is} = V_{SS}$ to $V_{DD}$ | | 5 | 800 | 850 | 1200 | 1300 | 470 | 1050 | Ω |
| | | | 10 | 310 | 330 | 500 | 550 | 180 | 400 | |
| | | | 15 | 200 | 210 | 300 | 320 | 125 | 240 | |
| ΔOn-State Resistance Between Any 2 Switches, $\Delta r_{on}$ | $R_L$=10 kΩ, $V_C = V_{DD}$ | | 5 | – | – | – | – | 15 | – | Ω |
| | | | 10 | – | – | – | – | 10 | – | |
| | | | 15 | – | – | – | – | 5 | – | |
| Total Harmonic Distortion, THD | $V_C$=$V_{DD}$ = 5 V, $V_{SS}$ = −5 V, $V_{is(p-p)}$ = 5 V (Sine wave centered on 0 V) $R_L$=10 kΩ, $f_{is}$=1 kHz sine wave | | | – | – | – | – | 0.4 | – | % |
| −3dB Cutoff Frequency (Switch on) | $V_C$=$V_{DD}$=5 V, $V_{SS}$ = −5 V, $V_{is(p-p)}$ =5 V (Sine wave centered on 0 V $R_L$ = 1 kΩ, | | | – | – | – | – | 40 | – | MHz |
| −50dB Feed-through Frequency (Switch off) | $V_C$=$V_{SS}$= −5 V, $V_{is(p-p)}$ = 5 V Sine wave centerd on 0 V $R_L$ = 1 kΩ | | | – | – | – | – | 1 | – | MHz |
| Input/Output Leakage Current (Switch off) $I_{is}$ Max. | $V_C$ = 0 V $V_{is}$ = 18 V; $V_{os}$ = 0 V, $V_{is}$ = 0V; $V_{os}$ = 18 V | | 18 | ±0.1 | ±0.1 | ±1 | ±1 | $±10^{-5}$ | ±0.1 | μA |
| −50 dB Crosstalk Frequency | $V_C$(A) = $V_{DD}$ = +5 V, $V_C$(B) = $V_{SS}$ = −5 V, $V_{is}$(A) = 5 $V_{p-p}$, 50 Ω source $R_L$ = 1 kΩ | | | – | – | – | – | 8 | – | MHz |
| Propagation Delay (Signal Input to Signal Output) $t_{pd}$ | $R_L$ = 200 kΩ $V_C$ = $V_{DD}$, $V_{SS}$ = GND, $C_L$ = 50 pF $V_{is}$ = 10 V (Square wave centered on 5 V $t_r$, $t_f$ = 20 ns | | 5 | – | – | – | – | 20 | 40 | ns |
| | | | 10 | – | – | – | – | 10 | 20 | |
| | | | 15 | – | – | – | – | 7 | 15 | |
| Capacitance: Input, $C_{is}$ | $V_{DD}$ = +5 V $V_C$ = $V_{SS}$ = −5 V | | | – | – | – | – | 8 | – | pF |
| Output, $C_{os}$ | | | | – | – | – | – | 8 | – | |
| Feedthrough, $C_{ios}$ | | | | – | – | – | – | 0.5 | – | |

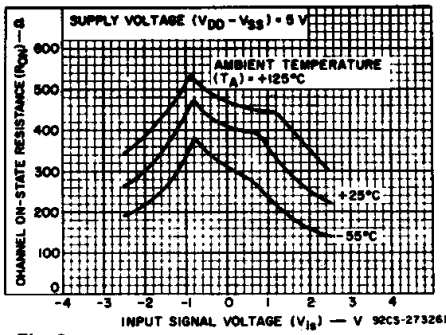



*Fig. 2— Typical on-state resistance vs. input signal voltage (all types).*

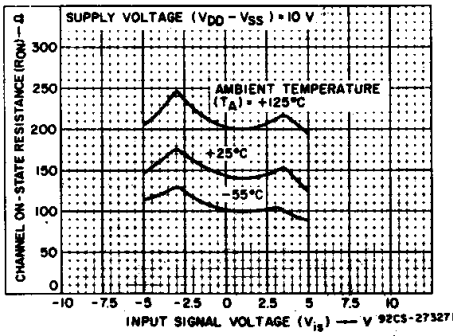



*Fig. 3— Typical on-state vs. input signal voltage (all types).*

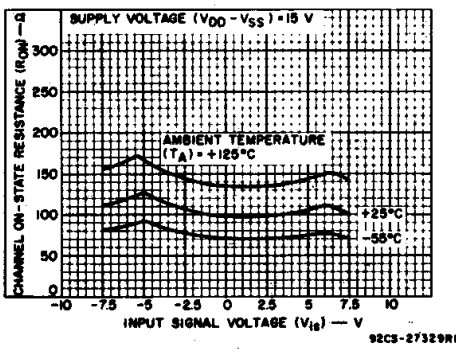



*Fig. 4— Typical on-state resistance vs. input signal voltage (all types).*

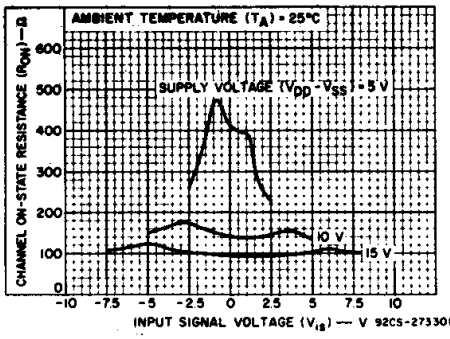



*Fig. 5— on-state resistance vs. input signal voltage (all types).*

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

ELECTRICAL CHARACTERISTICS (cont'd)

| CHARACTERISTIC | TEST CONDITIONS | $V_{DD}$ (V) | LIMITS AT INDICATED TEMPERATURES (°C) –55 | –40 | +85 | +125 | +25 Typ. | +25 Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **Control ($V_C$)** | | | | | | | | | |
| Control Input Low Voltage, $V_{ILC}$ Max. | $\|I_{is}\| < 10\mu A$, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$ and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$ | 5 | 1 | 1 | 1 | 1 | – | 1 | V |
| | | 10 | 2 | 2 | 2 | 2 | – | 2 | |
| | | 15 | 2 | 2 | 2 | 2 | – | 2 | |
| Control Input High Voltage, $V_{IHC}$ | See Fig. 6 | 5 | 3.5 (Min.) | | | | | | V |
| | | 10 | 7 (Min.) | | | | | | |
| | | 15 | 11 (Min.) | | | | | | |
| Input Current, $I_{IN}$ Max. | $V_{is} \leq V_{DD}$, $V_{DD} - V_{SS} = 18$ V, $V_{CC} \leq V_{DD} - V_{SS}$ | 18 | ±0.1 | ±0.1 | ±1 | ±1 | $\pm 10^{-5}$ | ±0.1 | μA |
| Crosstalk (Control Input to Signal Output) | $V_C$ = 10 V (Sq. Wave), $t_r$, $t_f$ = 20 ns, $R_L$ = 10 kΩ | 10 | – | – | – | – | 50 | – | mV |
| Turn-On and Turn-Off Propagation Delay | $V_{IN} = V_{DD}$, $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 1 kΩ | 5 | – | – | – | – | 35 | 70 | ns |
| | | 10 | – | – | – | – | 20 | 40 | |
| | | 15 | – | – | – | – | 15 | 30 | |
| Maximum Control Input Repetition Rate | $V_{is} = V_{DD}$, $V_{SS}$ = GND, $R_L$ = 1 kΩ to gnd, $C_L$ = 50 pF, $V_C$ = 10 V (Square wave centered on 5 V), $t_r$, $t_f$ = 20 ns, $V_{OS} = \frac{1}{2} V_{OS}$ @ 1 kHz | 5 | – | – | – | – | 6 | – | MHz |
| | | 10 | – | – | – | – | 9 | – | |
| | | 15 | – | – | – | – | 9.5 | – | |
| Input Capacitance, $C_{IN}$ | | | – | – | – | – | 5 | 7.5 | pF |

| $V_{DD}$ (V) | $V_{is}$ (V) | Switch Input $I_{is}$ (mA) –55°C | –40°C | +25°C | +85°C | +125°C | Switch Output, $V_{OS}$ (V) Min. | Max. |
|---|---|---|---|---|---|---|---|---|
| 5 | 0 | 0.64 | 0.61 | 0.51 | 0.42 | 0.36 | – | 0.4 |
| 5 | 5 | –0.64 | –0.61 | –0.51 | –0.42 | –0.36 | 4.6 | – |
| 10 | 0 | 1.6 | 1.5 | 1.3 | 1.1 | 0.9 | – | 0.5 |
| 10 | 10 | –1.6 | –1.5 | –1.3 | –1.1 | –0.9 | 9.5 | – |
| 15 | 0 | 4.2 | 4 | 3.4 | 2.8 | 2.4 | – | 1.5 |
| 15 | 15 | –4.2 | –4 | –3.4 | –2.8 | –2.4 | 13.5 | – |

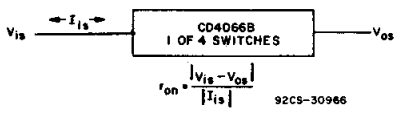



*Fig. 6— Determination of $r_{on}$ as a test condition for control input high voltage ($V_{IHC}$) specification.*

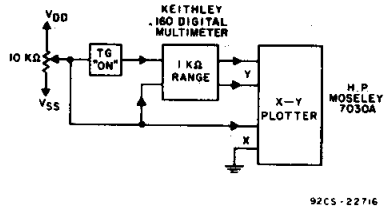



*Fig. 7 — Channel on-state resistance measurement circuit.*

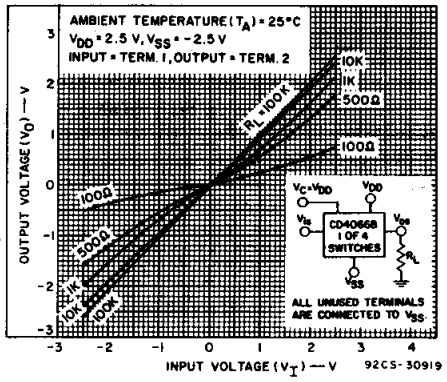



*Fig. 8—Typical ON characteristics for 1 of 4 Channels.*

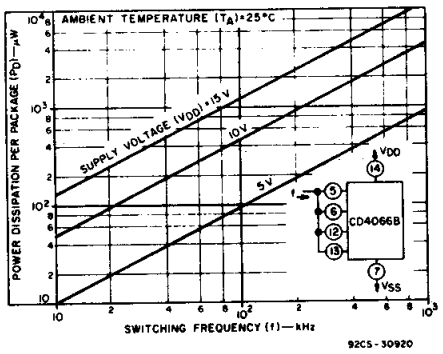



*Fig. 9 — Power dissipation per package vs. switching frequency.*

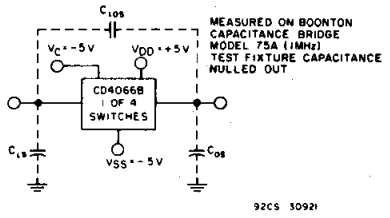



*Fig. 10 — Capacitance test circuit.*

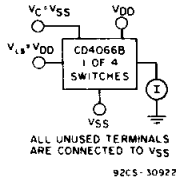



Fig. 11 – Off-switch input or output leakage.

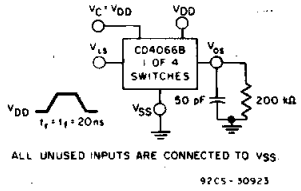



Fig. 12 – Propagation delay time signal input ($V_{is}$) to signal output ($V_{os}$).

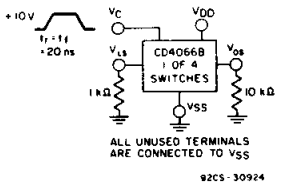



Fig. 13 – Crosstalk-control input to signal output.

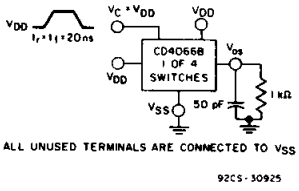



Fig. 14 – Propagation delay $t_{PLH}$, $t_{PHL}$ control-signal output. Delay is measured at $V_{OS}$ level of +10% from ground (turn-on) or on-state output level (turn-off).

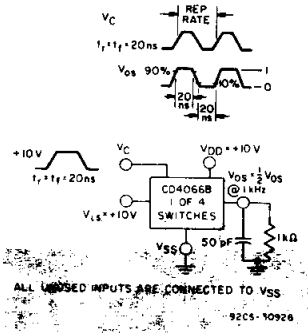



Fig. 15 – Maximum allowable control input repetition rate.

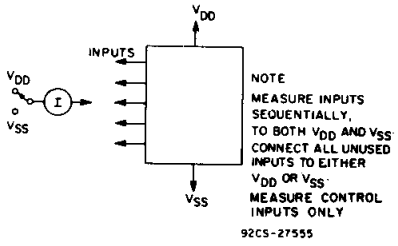



Fig. 16 – Input leakage current test circuit.

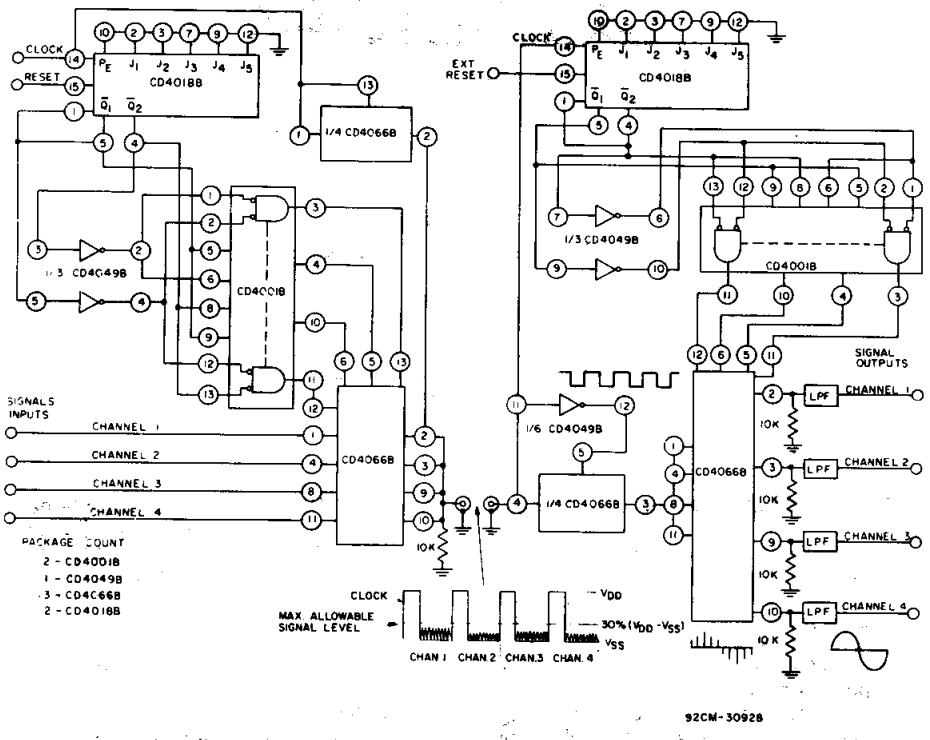



Fig. 17– 4-channel PAM multiplex system diagram.

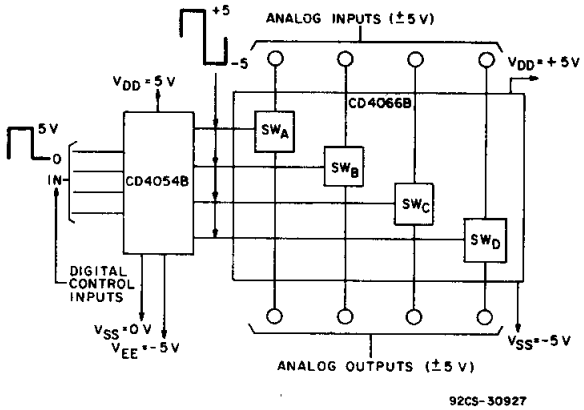
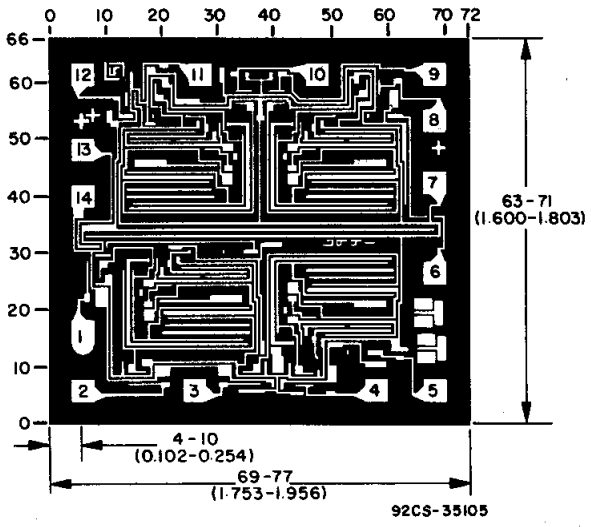



*Fig. 18 – Bidirectional signal transmission via digital control logic.*




**CD4066BH**
**CHIP DIMENSIONS AND PAD LAYOUT**

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

**SPECIAL CONSIDERATIONS — CD4066B**

1. In applications that employ separate power sources to drive $V_{DD}$ and the signal inputs, the $V_{DD}$ current capability should exceed $V_{DD}/R_L$ ($R_L$ = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the $V_{DD}$ supply when power is applied or removed from the CD4066B.
2. In certain applications, the external load-resistor current may include both $V_{DD}$ and signal-line components. To avoid drawing $V_{DD}$ current when switch current flows into terminals 1,4,8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from $R_{ON}$ values shown).

   No $V_{DD}$ current will flow through $R_L$ if the switch current flows into terminals 2,3,9, or 10.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265