

Distributed by:



**[www.Jameco.com](http://www.Jameco.com) ♦ 1-800-831-4242**

The content and copyrights of the attached  
material are the property of its owner.

Jameco Part Number 12079ISL

## General Purpose NPN Transistor Array

The CA3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

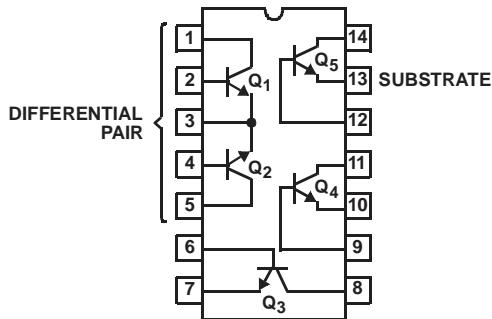
The transistors of the CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

## Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3046	-55 to 125	14 Ld PDIP	E14.3
CA3046M (3046)	-55 to 125	14 Ld SOIC	M14.15
CA3046M96 (3046)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

## Pinout

CA3046 (PDIP, SOIC)  
TOP VIEW



## Features

- Two Matched Transistors
  - $V_{BE}$  Match .....  $\pm 5\text{mV}$
  - $I_{IO}$  Match .....  $2\mu\text{A}$  (Max)
- Low Noise Figure ..... 3.2dB (Typ) at 1kHz
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120MHz
- Wide Operating Current Range
- Full Military Temperature Range

## Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

**Absolute Maximum Ratings**

Collector-to-Emitter Voltage ( $V_{CEO}$ )	15V
Collector-to-Base Voltage ( $V_{CBO}$ )	20V
Collector-to-Substrate Voltage ( $V_{CIO}$ , Note 1)	20V
Emitter-to-Base Voltage ( $V_{EBO}$ )	5V
Collector Current ( $I_C$ )	50mA

**Operating Conditions**

Temperature Range	-55°C to 125°C
-------------------	----------------

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTES:

1. The collector of each transistor of the CA3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $T_A = 25^\circ\text{C}$ , characteristics apply for each transistor in CA3046 as specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
<b>DC CHARACTERISTICS</b>							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu\text{A}$ , $I_E = 0$		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{mA}$ , $I_B = 0$		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu\text{A}$ , $I_{CI} = 0$		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu\text{A}$ , $I_C = 0$		5	7	-	V
Collector Cutoff Current (Figure 1)	$I_{CBO}$	$V_{CB} = 10\text{V}$ , $I_E = 0$		-	0.002	40	nA
Collector Cutoff Current (Figure 2)	$I_{CEO}$	$V_{CE} = 10\text{V}$ , $I_B = 0$		-	See Fig. 2	0.5	μA
Forward Current Transfer Ratio (Static Beta) (Note 3) (Figure 3)	$h_{FE}$	$V_{CE} = 3\text{V}$	$I_C = 10\text{mA}$	-	100	-	-
			$I_C = 1\text{mA}$	40	100	-	-
			$I_C = 10\mu\text{A}$	-	54	-	-
Input Offset Current for Matched Pair $Q_1$ and $Q_2$ , $ I_{O1} - I_{O2} $ (Note 3) (Figure 4)		$V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	0.3	2	μA
Base-to-Emitter Voltage (Note 3) (Figure 5)	$V_{BE}$	$V_{CE} = 3\text{V}$	$I_E = 1\text{mA}$	-	0.715	-	V
			$I_E = 10\text{mA}$	-	0.800	-	V
Magnitude of Input Offset Voltage for Differential Pair $ V_{BE1} - V_{BE2} $ (Note 3) (Figures 5, 7)		$V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $ V_{BE3} - V_{BE4} $ , $ V_{BE4} - V_{BE5} $ , $ V_{BE5} - V_{BE3} $ (Note 3) (Figures 5, 7)		$V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	-1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	$V_{CES}$	$I_B = 1\text{mA}$ , $I_C = 10\text{mA}$		-	0.23	-	V
Temperature Coefficient: Magnitude of Input Offset Voltage (Figure 7)	$\frac{ \Delta V_{IO} }{\Delta T}$	$V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	1.1	-	μV/°C
<b>DYNAMIC CHARACTERISTICS</b>							
Low Frequency Noise Figure (Figure 9)	NF	$f = 1\text{kHz}$ , $V_{CE} = 3\text{V}$ , $I_C = 100\mu\text{A}$ , Source Resistance = $1\text{k}\Omega$		-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics							
Forward Current Transfer Ratio (Figure 11)	$h_{FE}$	$f = 1\text{kHz}$ , $V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	110	-	-
Short Circuit Input Impedance (Figure 11)	$h_{IE}$	$f = 1\text{kHz}$ , $V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 11)	$h_{OE}$	$f = 1\text{kHz}$ , $V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$		-	15.6	-	μS

**Electrical Specifications**  $T_A = 25^\circ\text{C}$ , characteristics apply for each transistor in CA3046 as specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Circuit Reverse Voltage Transfer Ratio (Figure 11)	$h_{RE}$	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	-	$1.8 \times 10^{-4}$	-	-
Admittance Characteristics						
Forward Transfer Admittance (Figure 12)	$Y_{FE}$	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	-	$31 - j1.5$	-	-
Input Admittance (Figure 13)	$Y_{IE}$	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	-	$0.3 + j0.04$	-	-
Output Admittance (Figure 14)	$Y_{OE}$	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	-	$0.001 + j0.03$	-	-
Reverse Transfer Admittance (Figure 15)	$Y_{RE}$	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	-	See Fig. 14	-	-
Gain Bandwidth Product (Figure 16)	$f_T$	$V_{CE} = 3\text{V}, I_C = 3\text{mA}$	300	550	-	MHz
Emitter-to-Base Capacitance	$C_{EB}$	$V_{EB} = 3\text{V}, I_E = 0$	-	0.6	-	pF
Collector-to-Base Capacitance	$C_{CB}$	$V_{CB} = 3\text{V}, I_C = 0$	-	0.58	-	pF
Collector-to-Substrate Capacitance	$C_{CI}$	$V_{CS} = 3\text{V}, I_C = 0$	-	2.8	-	pF

NOTE:

3. Actual forcing current is via the emitter for this test.

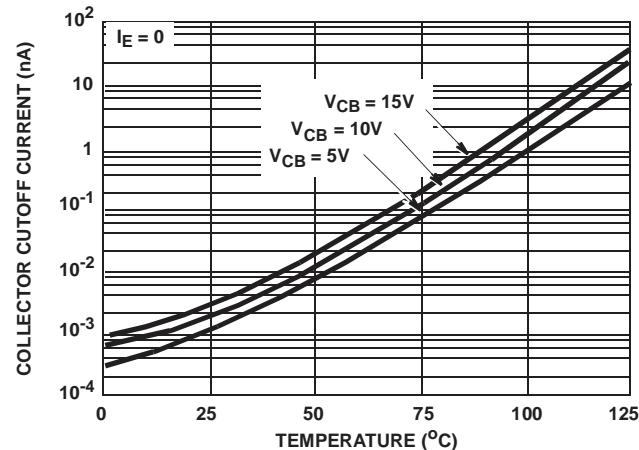
**Typical Performance Curves**

FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

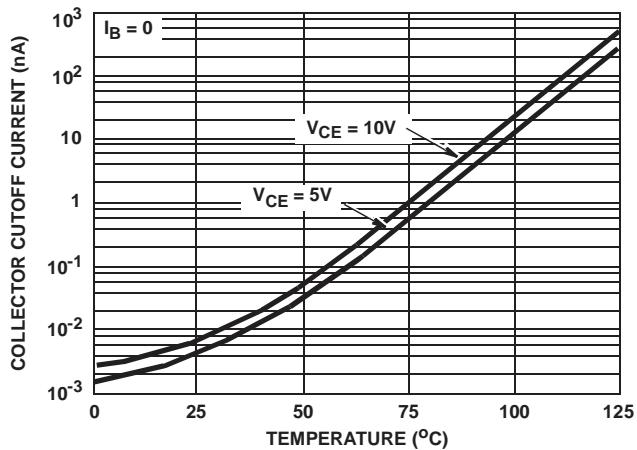


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

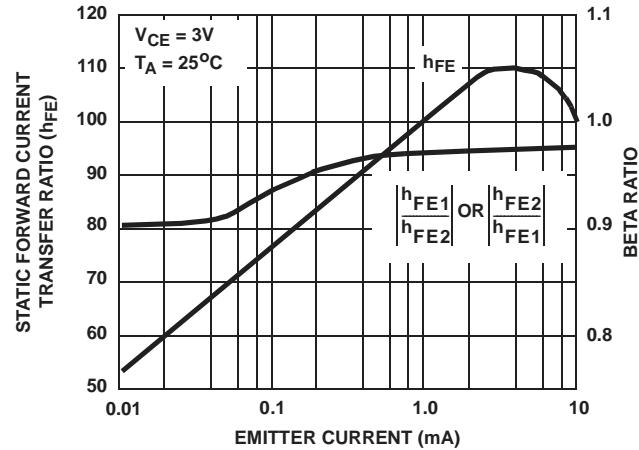


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR Q<sub>1</sub> AND Q<sub>2</sub> vs Emitter Current

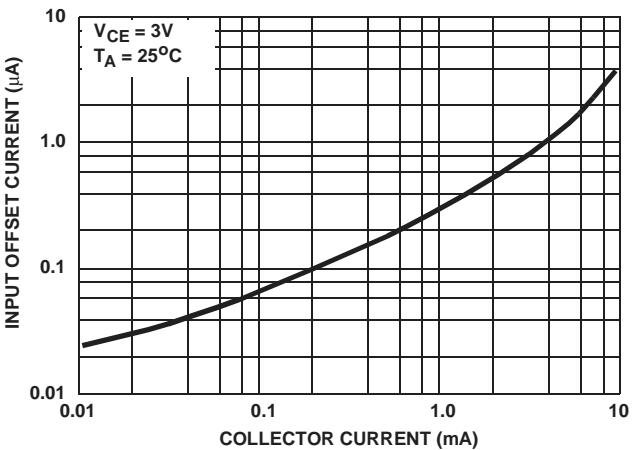


FIGURE 4. TYPICAL INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q<sub>1</sub>Q<sub>2</sub> vs COLLECTOR CURRENT

## Typical Performance Curves (Continued)

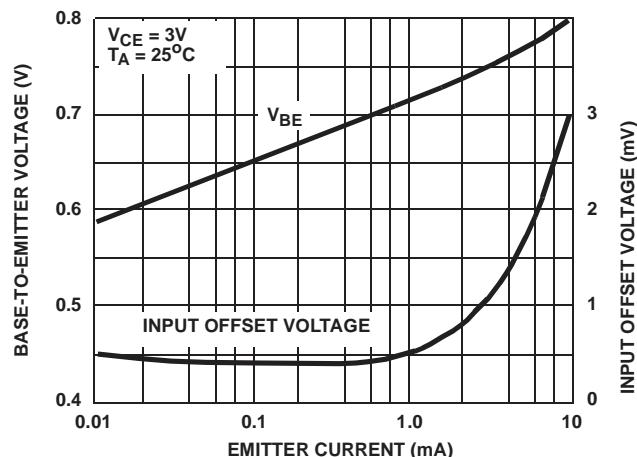


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTICS AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs Emitter Current

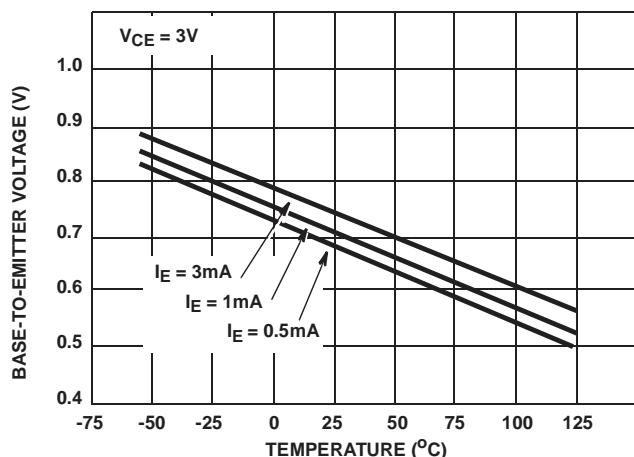


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC vs TEMPERATURE FOR EACH TRANSISTOR

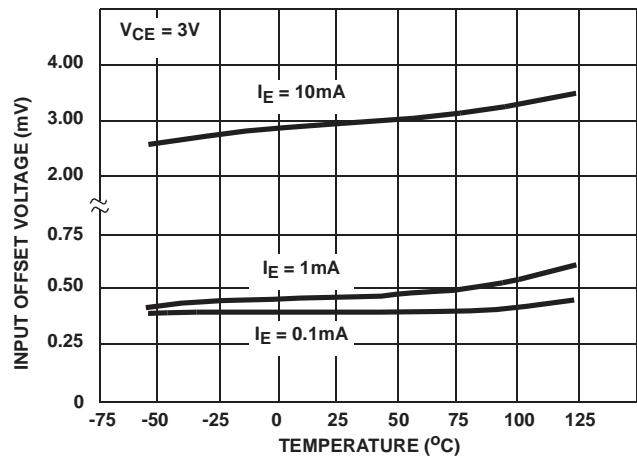


FIGURE 7. TYPICAL INPUT OFFSET VOLTAGE CHARACTERISTICS FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs TEMPERATURE

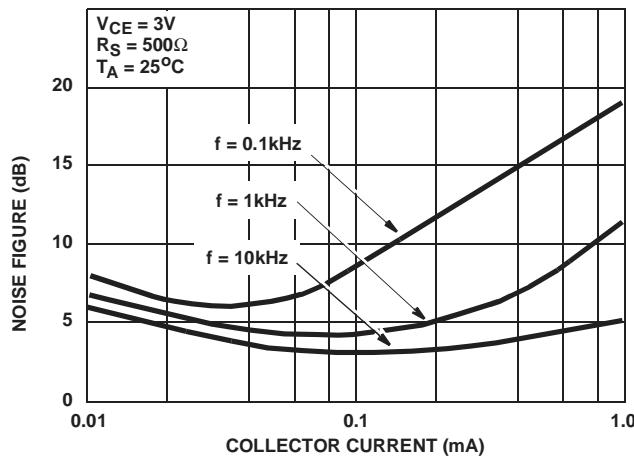


FIGURE 8. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

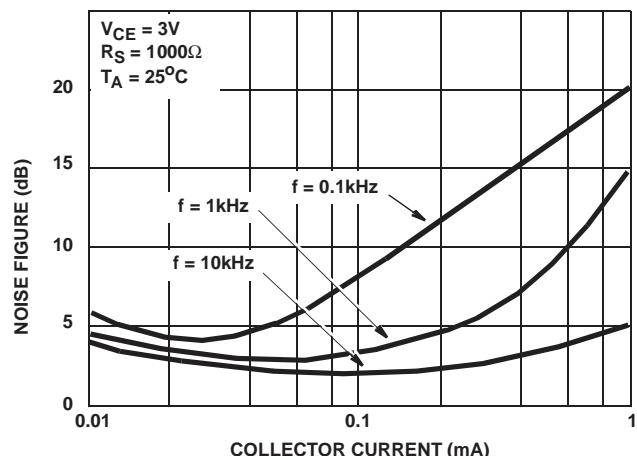


FIGURE 9. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

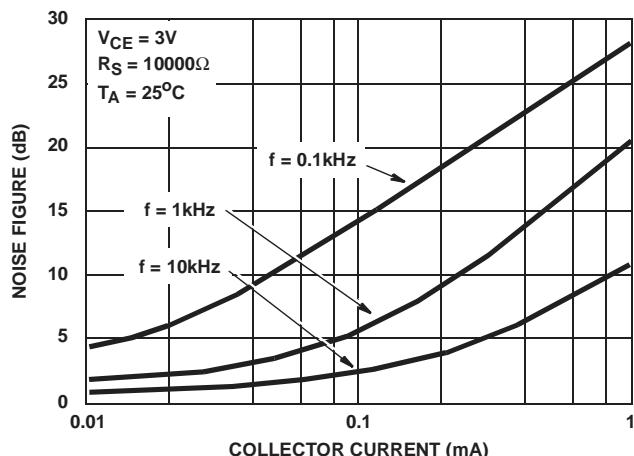


FIGURE 10. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

## Typical Performance Curves (Continued)

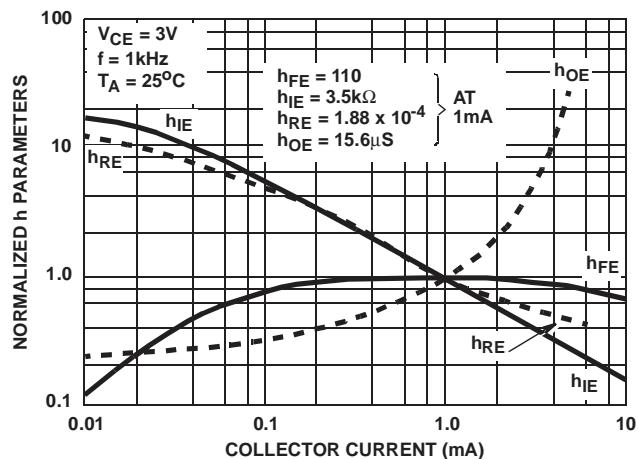


FIGURE 11. TYPICAL NORMALIZED FORWARD CURRENT TRANSFER RATIO, SHORT CIRCUIT INPUT IMPEDANCE, OPEN CIRCUIT OUTPUT IMPEDANCE, AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO vs COLLECTOR CURRENT

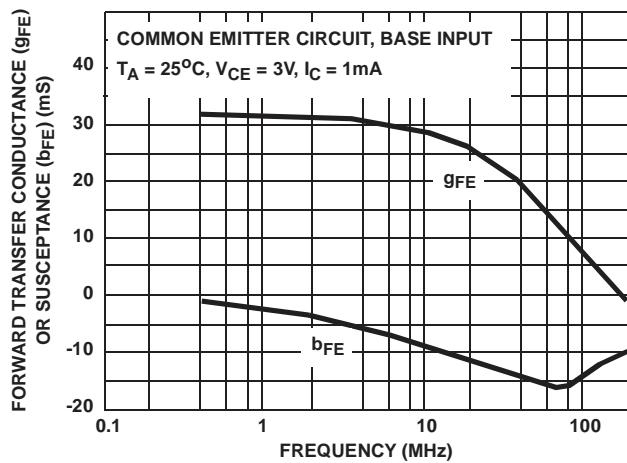


FIGURE 12. TYPICAL FORWARD TRANSFER ADMITTANCE vs FREQUENCY

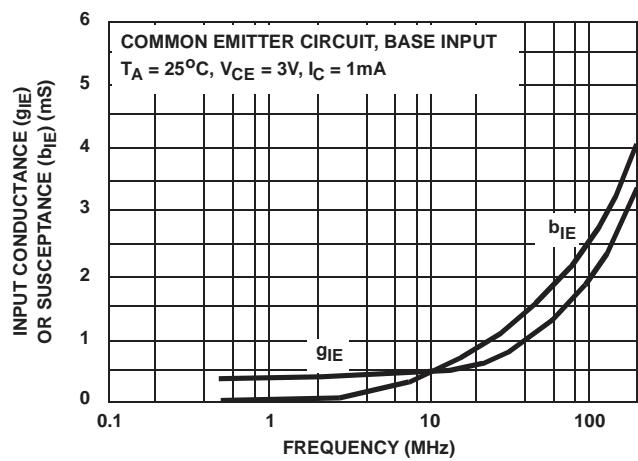


FIGURE 13. TYPICAL INPUT ADMITTANCE vs FREQUENCY

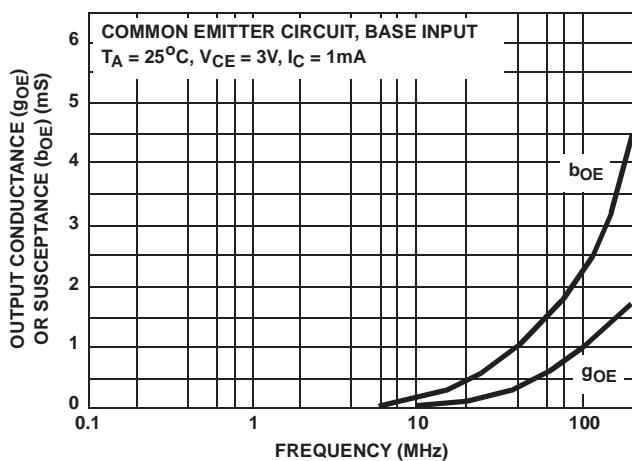


FIGURE 14. TYPICAL OUTPUT ADMITTANCE vs FREQUENCY

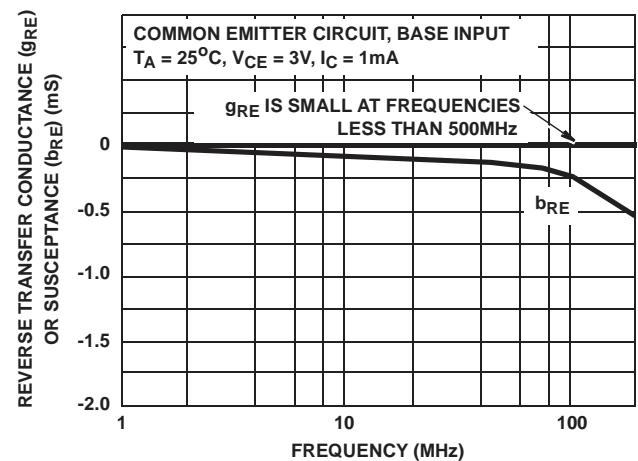


FIGURE 15. TYPICAL REVERSE TRANSFER ADMITTANCE vs FREQUENCY

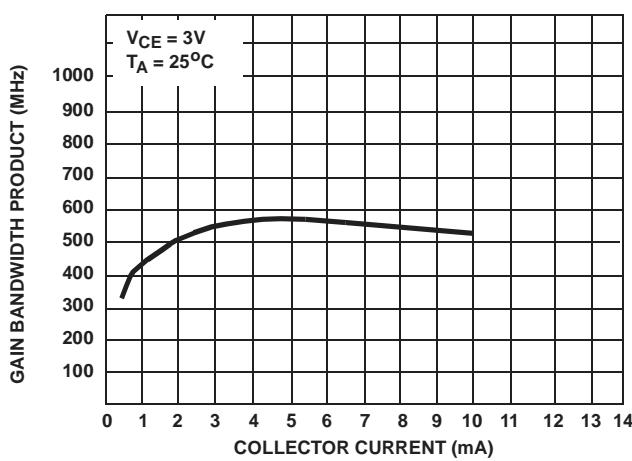


FIGURE 16. TYPICAL GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

All Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at website [www.intersil.com/design/quality/iso.asp](http://www.intersil.com/design/quality/iso.asp).

---

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

---

For information regarding Intersil Corporation and its products, see web site [www.intersil.com](http://www.intersil.com)

### **Sales Office Headquarters**

#### **NORTH AMERICA**

Intersil Corporation  
2401 Palm Bay Rd.  
Palm Bay, FL 32905  
TEL: (321) 724-7000  
FAX: (321) 724-7240

#### **EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusée  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

#### **ASIA**

Intersil Ltd.  
8F-2, 96, Sec. 1, Chien-kuo North,  
Taipei, Taiwan 104  
Republic of China  
TEL: 886-2-2515-8508  
FAX: 886-2-2515-8369